

Digital based calibration technique for continuous-time bandpass sigma-delta analog-to-digital converters

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Abstract In this paper, a calibration technique for Noise Transfer Function (NTF) optimization of Continuous-Time Bandpass Sigma Delta (CT BP $\Sigma\Delta$) modulators is presented. The proposed technique employs a test tone applied at the input of the quantizer to evaluate the noise transfer function of the Analog-to-Digital Converter (ADC) using the capabilities of the Digital Signal Processing (DSP) platform usually available in mixed-mode systems. Once the ADC output bit stream is captured, necessary information to generate the control signals to tune the ADC parameters for best Signal-to-Quantization Noise Ratio (SQNR) performance is extracted via an LMS software-based algorithm. Simulation results show that notch frequency of the NTF due to process variations and temperature tolerances can be tuned using the proposed methodology. The proposed global calibration approach can be used during the system start-up and the idle system time. The proposed approach uses a single in-band calibration tone, but it can be expanded using out-of band test tones for background calibration schemes.

Keywords Bandpass sigma-delta modulators · ADC calibration techniques · Continuous-time · Bandpass modulators · Sigma-delta modulators

1 Introduction

With the increasing number of services and wireless standards in the last decade, the next generation of communication solutions must support fully-integrated systems on a chip (SoC) in order to advance towards the design of multi-standard CMOS devices. Following this trend, the emphasis of the new transceivers is to perform the broadband signal processing to accommodate higher data throughput. A major building block in multi-standard high-speed transceivers is the ADC. For RF and high-IF solutions, Continuous-Time Bandpass $\Sigma\Delta$ Modulators (CT-BP) are frequently used because at high intermediate frequencies the flicker noise is small compared to that of the quantization noise [1–3]. A major issue found in continuous-time networks is the lack of accuracy due to process-voltage temperature tolerances that may lead to over 25% variations on the time constants [1, 4, 5]. To alleviate this problem, the master-slave tuning techniques have been successfully used in continuous-time filters; this approach, however, has been accompanied by additional calibration schemes since tuning the loop filter is not enough to guarantee the best operation of the entire ADC loop [1, 7, 8]. The optimally tuned ADC requires correcting for filter's center frequency deviations, excess loop delays and variations of DAC coefficients. These issues are partially alleviated by optimizing the architecture using double delay resonators and feedforward techniques [6]. Another approach measures in the digital domain the notch performance of ADC [7]; this approach is however affected by the power of the incoming out-of band information in on-line calibration schemes but it is an interesting approach for off-line calibration. Optimization of individual building blocks and use of programmable delay lines for the optimization of the loop delay and reconfigurable filter-oscillator system for

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notch tuning were also reported in [8]. This approach tunes the ADC parameters at the powering up.

The off-line software based loop calibration technique introduced in this letter is intended for the optimization of the noise transfer function in bandpass sigma-delta modulators, and can be used during the system calibration times. The proposed approach measures the noise transfer function in digital domain using an auxiliary and non-critical test tone; based on the response of the loop to the strategically applied tone, the loop parameters are sequentially adjusted until the noise transfer function presents its best possible performance. The main concept introduced in this paper uses a single in-band test tone suitable for off-line calibration, but the approach can be exported to on-line calibration.

2 The CT sigma-delta modulator

Figure 1 shows a block diagram of a typical CT BP $\Sigma\Delta$ Modulator using a 4th order BP filter and a multi-bit quantizer. Assuming a unity gain quantizer, it can be shown that the Signal Transfer Function (STF) and the quantization Noise Transfer Function (NTF) can be approximated as

$$STF(s) = \frac{\omega_o^2 \left(s + \frac{\omega_o}{2Q}\right)^2}{\left(s^2 + \frac{\omega_o}{Q}s + \omega_o^2\right)^2 + (\omega_o^2\beta) \left(s + \frac{\omega_o}{2Q}\right)^2} \quad (1)$$

$$NTF(s) = \frac{\left(s^2 + \frac{\omega_o}{Q}s + \omega_o^2\right)^2}{\left(s^2 + \frac{\omega_o}{Q}s + \omega_o^2\right)^2 + (\omega_o^2\beta) \left(s + \frac{\omega_o}{2Q}\right)^2} \quad (2)$$

where β is the gain of the feedback DAC; ω_o and Q are filter’s center frequency and pole’s finite quality factor, respectively. At the resonant frequency ($\omega = \omega_o$) and assuming high- Q sections, these equations simplify to

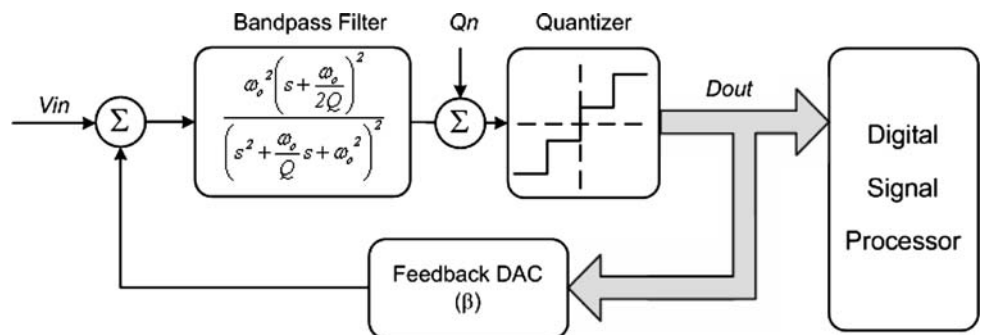
$$STF(s) = \frac{\left(j + \frac{1}{2Q}\right)^2}{-\left(\frac{1}{Q}\right)^2 + (\beta) \left(j + \frac{1}{2Q}\right)^2} \cong \frac{1}{\beta} \quad (3)$$

$$NTF(s) = \frac{-1}{-1 + (\beta) \left(jQ + \frac{1}{2}\right)^2} \cong \frac{1}{\beta Q^2} \quad (4)$$

Assuming ideal components the Q factor can be made very large, and the magnitude of the NTF evaluated at the resonant frequency $s = j\omega_o$ becomes very small, which leads to an excellent SQNR performance around the resonant frequency. However, ω_o in continuous-time filters typically changes by $\pm 25\%$ over process-voltage-temperature (PVT) variations. Also, a finite gain of <30 dB in single stage amplifiers and parasitic poles in high-gain amplifiers will limit the Q factor of high-frequency filters, which reduces the ADC’s SQNR because at ω around ω_o the shape of the NTF given in (4) strongly depends on Q and β . In addition, the excess loop delay between the quantizer sampling time and the time when a change in the output bit is seen at the feedback point in the filter will cause SNR degradation and stability issues. Excess loop delay has to be limited to no more than 10% of the clock period in order not to degrade the SQNR [9]. Also, it has been reported in previous publications that 0.1% and 0.4% RMS clock jitter reduces ADC’s SQNR by over 1 dB and 10 dB, respectively. Fortunately, state of the art clock generators using on-chip PLLs can reduce the RMS clock jitter to the range of 1 psec, enabling the use of clocks in the range of 1 GHz.

The global calibration strategy described in the following section takes into account all PVT variations, DAC coefficient accuracy and excess loop delay to effectively optimize ADC’s loop performance. The proposed strategy is not able to correct DAC non-linearities which may require the use of randomization techniques such as dynamic element matching.

Fig. 1 Simplified block diagram of a continuous-time 4th order bandpass sigma-delta modulator



3 Proposed calibration technique

The proposed loop calibration approach relies on a software-based platform instead of power hungry and inaccurate analog circuitry. The system level implementation of the proposed digital based tuning scheme for the CT-BP $\Sigma\Delta$ ADC is shown in Fig. 2. In addition to a non-critical out-of band analog input signal, a test tone at the desired center frequency ω_o is applied at the input of the quantizer to emulate a systematic and testable in-band quantization noise. Since the test tone is applied at the output of the loop, its noise is shaped by loop transfer function and the auxiliary circuitry has very little effect on the dynamics of the loop. The quantizer output digital bit stream is then processed by the digital signal processor (DSP), and the power of the test tone is then measured in the digital domain using the Fast Fourier transform (FFT). The estimated power of the test tone is used in an adaptive Least Mean Square (LMS) algorithm that controls several parameters with the aim of minimizing the power of the measured test tone and thus maximizing the rejection to quantization noise. The LMS algorithm generates the digital control signals to tune loop's notch frequency by controlling a bank of capacitors used for the realization of the bandpass filter. Once the notch frequency of the NTF is set at the desired frequency, the DAC coefficients and excess loop delay are then adjusted with the same aim: power minimization of the test tone to reach the best possible signal to quantization noise ratio.

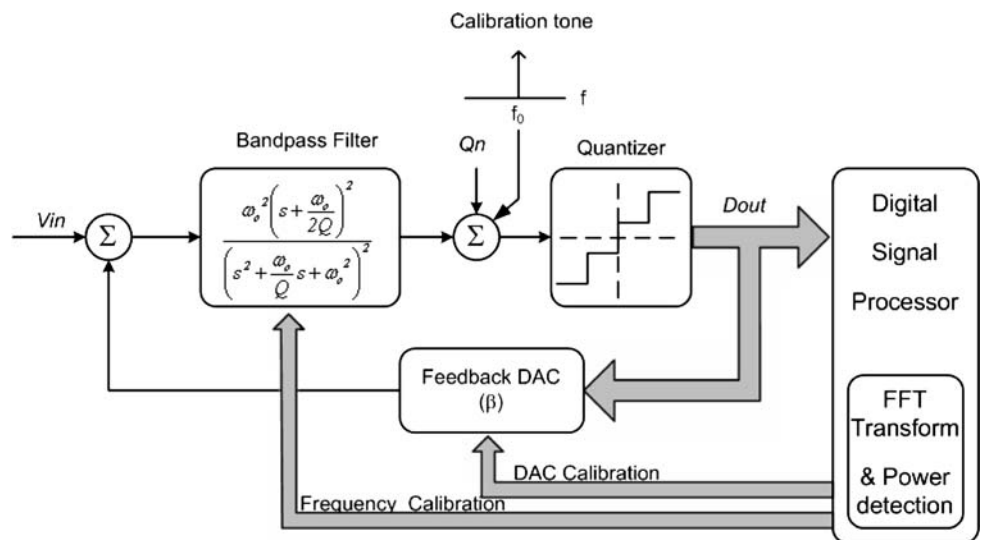
The algorithm for the digital tuning scheme is described by the following steps: (i) Inject a test tone signal at the desired frequency at the quantizer input; (ii) inject an input signal such that the loop operates properly, frequency and power of this signal is not relevant for the operation of the

calibration algorithm; (iii) find the frequency component of the test tone frequency and store their value in digital format; (iv) by means of a LMS algorithm a digital control tuning signal is computed based on the difference between the stored and the new estimated power value of the detected test tone; (v) the parameters that control ω_o are tuned first; (vi) iterate between (iii) and (v) until the power of the measured test tone is minimized; (vii) Once the frequency of the NTF notch is tuned, the algorithm tunes the DAC coefficients and a programmable delay element, if required, until the power of the detected test tone is minimized. The algorithm ensures that at the end of the process the critical loop parameters are tuned for the best SQNR.

4 Simulated results

The strength of the test tone is not critical; it can be very small but it must be well above the noise floor to be easily detected. Also, a non-critical input signal around but not at the center frequency can be injected at the input of the modulator to ensure that the loop is operating properly. Figure 3 shows the response of the un-calibrated $f_s/4$ 4th order 200 MHz ADC to two tones. The first one is applied at the input of the ADC at 210 MHz; the calibration tone is applied at the input of the quantizer at the desired 200 MHz frequency and used for the calibration of the NTF. Over 25% variations on the loop parameters were intentionally introduced; this results in a notch's frequency around 250 MHz instead of 200 MHz. After several iterations using the aforementioned algorithm, the loop notch's frequency is tuned to the desired value by just monitoring the power of the test tone set at 200 MHz and adjusting the bank of capacitors used in the loop filter for that purpose.

Fig. 2 Continuous-time 4th order bandpass sigma-delta modulator with frequency and DAC calibration



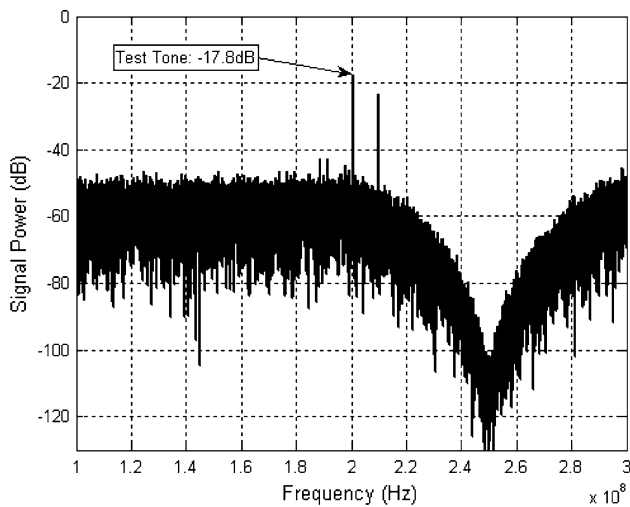


Fig. 3 Output spectrum for the un-calibrated loop: PVT variations are over 25%; power of test tone centered at 200 MHz is -18 dB

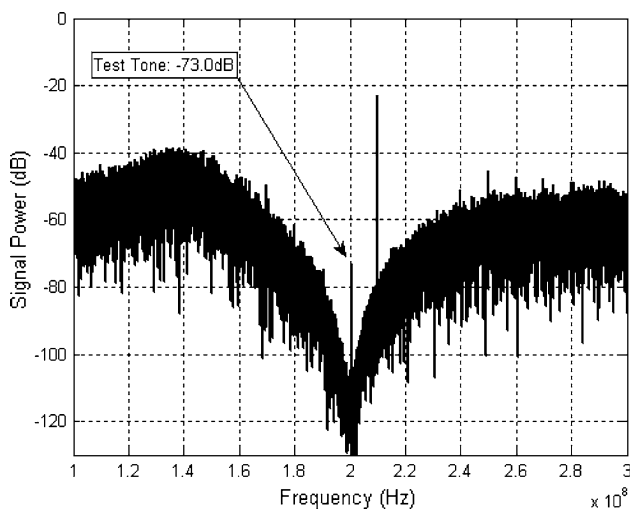


Fig. 4 Output spectrum after calibration: power of calibration tone centered at 200 MHz is -65 dB. Power of the applied test tone is -10 dB, leading to a quantization noise gain at the center frequency of -45 dB after calibration

Figure 4 shows the ADC spectrum after calibration. The algorithm stops when the power of the tone at quantizer output is at its minimum value; e.g. -65 dB at the output while the power of the test tone applied to the quantizer input is -10 dB. Once the loop's notch frequency is tuned, there is room for additional (usually 3–9 dB) SQNR improvement by fine tuning DAC coefficients and excess loop delay.

Since the loop tuning approach relies on power estimation in software and on the well controlled frequency of the test tone, the algorithm is quite robust and ensures the optimization of the most critical parameter in the bandpass ADCs: the noise transfer function. Notice in Eq. 3 and

Figs. 3 and 4 that the power of the tone applied at the analog input of the ADC at 210 MHz is almost insensitive to the tuning of the loop parameters, suggesting that it is very difficult to calibrate the ADC loop by injecting testing signals at the ADC's input. This result is expected since the closed loop gain is close to unity in the band where filter's gain is large.

5 Conclusion

A software-based calibration scheme intended for continuous-time bandpass sigma-delta modulators has been proposed. The technique requires a test tone at the desired center frequency; while tone's power is not critical, it is desirable to limit its power to 10 dB below the maximum input power tolerated by the ADC to ensure that the quantizer is not saturated. The proposed technique requires extensive digital computation since the power of the calibration tone must be extracted through FFT, but this is not a major drawback since digital processing is well suited for current and future deep-submicron technologies wherein digital circuitry is becoming faster and cheaper.

The calibration technique can be used at the power start-up or during the idle system times. Although the proposed technique is demonstrated using a single in-band calibration tone, it can be expanded to the use of out-of band testing tones for background calibration schemes.

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