

Robust derivative superposition method for linearising broadband LNAs

H.M. Geddada, J.W. Park and J. Silva-Martinez

A linearisation methodology for broadband low noise amplifiers (LNAs) is considered. The proposed scheme is composed of the main transistor operating in strong inversion healed by a couple of auxiliary transistors operating in triode and subthreshold regions. The nonlinearities of these transistors graciously and efficiently compensate each other, improving main transistor linearity by over 10 dB over all corners for input signals as large as -14 dBm. Power consumption increases by 6% while frequency response and input impedance are almost not affected because the compensating circuits are quite small compared with the main device. Simulation results show that the compensated LNA implemented in Jazz-Semiconductor 0.18 μm CMOS technology has a gain of 11.3 dB, IIP3 = 18.4 dBm, BW = 3.6 GHz while drawing 7.4 mA from a 2.4 V supply voltage.

Introduction: Wideband multi-standard front-ends are attractive for their reusability and low cost. However, the multi-standard front-ends require low noise figures and extremely high linearity for wide frequency range owing to the huge amount of input signal power as a result of the contribution of each one of the multiple services offered. Wideband multi-standard low noise amplifiers (LNAs) can be implemented using deep submicron CMOS technologies; the most popular topologies are based on common-source [1], common-gate [2] and resistive shunt and series feedback [3] configurations. Although the thermal noise level and the bandwidth of deep submicron CMOS technologies improve as transistor channel length decreases, transistor linearity gradually degrades owing to short-channel effects and the use of lower power supplies.

Many linearisation techniques for broadband amplifiers have been proposed over the last few years. A FET can be linearised by biasing at a gate-source voltage (V_{GS}) at which the third-order derivative of its DC transfer characteristic is zero [4–7]. High third-order input intermodulation distortion products (IIP3) can be achieved only in the neighbourhood of the bias point usually called ‘soft spot’; e.g. linearity improves for signal power under -25 dBm. In addition, this linearisation method is very sensitive to process and temperature variations. To reduce the IIP3 sensitivity to bias, the derivative superposition (DS) method was proposed in [8–9]. It employs multiple gated parallel (auxiliary) FETs of different widths and gate biases to achieve a composite DC transfer characteristic with an extended range in which the third-order derivative is close to zero. These auxiliary transistors biased in the subthreshold region add higher-order harmonic components because they turn on and off for large voltage swings. It is, however, difficult to achieve high linearity figures for all technology corners and temperature variations. Other techniques have also been reported [9–12]. Most of the linearisation schemes reported are very sensitive to PVT variations.

In this Letter, it is shown that by exploiting the inherent high f_t of deep submicron transistors and the proposed techniques based on the derivative superposition method, highly linear figures can be achieved for broadband LNAs. Two small transistors operating in the triode and the subthreshold region efficiently compensates main LNA nonlinearity. The healed LNA outperforms typical LNA linearity by over 10 dB for input signals as high as -14 dBm. Besides improving the linearity, the scheme is very robust to PVT variations.

Proposed LNA linearisation scheme: To simplify the test-bed, the conventional common-source cascode LNA shown in Fig. 1 is used. The noise figure is greater than 3 dB as it has a grounded $50\ \Omega$ resistive termination for impedance matching; this is not an issue in this work since the purpose is to show the properties of the proposed linearisation technique. Usually IIP3 figures around 0–10 dBm can be achieved for this topology. Fig. 2 shows the proposed LNA architecture; the setup includes the grounded input resistance of $50\ \Omega$ for impedance matching purposes. M0 is the baseline LNA with the same specifications as the baseline amplifier shown in Fig. 1. It has already been shown in previous publications that for a large enough bias current (>1 mA) the third-order variation of the current ($d^3i_d/dV_{GS}^3 = d^2gm/V_{GS}^2 = gm''$) in a saturated transistor is negative as depicted in the simulated results shown at the bottom trace of Fig. 3. Notice that the curvature of gm'' decreases for large drain currents. On the other hand, gm'' for a triode

biased transistor, MT, is positive as shown in the middle trace of Fig. 3. Another remarkable property of the transistor operating in the triode region is that the curvatures of gm'' for both transistors M0 and MT oppose each other, allowing nonlinearity cancellation for large signals when the current of both transistors are combined; this is one of the main transistor properties exploited in the proposed scheme and previously exploited in power amplifiers [13]. M2 serves two purposes: to fix the VDS voltage of MT to ensure its operation in the triode region and to avoid LNA gain degradation owing to the finite output resistance of MT. The bias current, I_{b2} is around 5% of I_{b1} ; hence power consumption penalty is affordable.

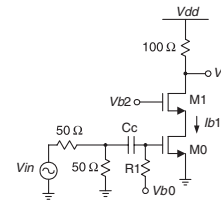


Fig. 1 Typical broadband common-source LNA with resistive matching

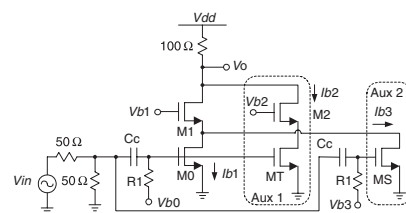


Fig. 2 Simplified schematic of compensated LNA

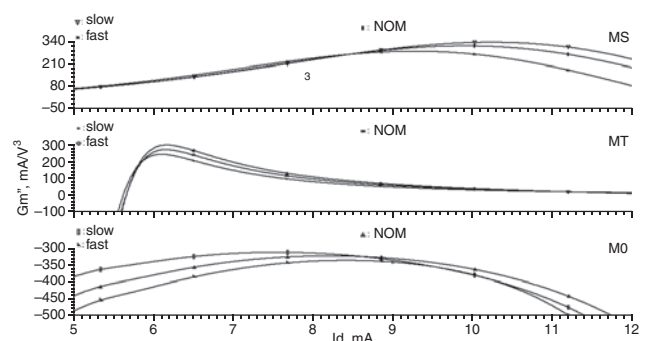


Fig. 3 gm'' variations over corners for M0, MT, MS

Unfortunately MT is not enough to fully cancel M0 nonlinearity; it is possible to match nonlinearity curvature but not its absolute value unless both bias current and transistor dimensions are further increased. Better nonlinearity cancellations are obtained if another transistor, MS, operating in the subthreshold region is added. As shown in the top trace of Fig. 3, if biased before the sweet spot its gm'' is positive. After combining the current of M0, MT and MS, the three nonlinearities gracefully cancel each other, leading to a robust wide linear range. An important design aspect in this scheme is that the delays from the main circuit path and the auxiliary paths must be identical at RF frequencies such that the nonlinearity cancellation is carried out with enough accuracy at the desired frequency range. Dimensions and bias current of the auxiliary transistors MT, M2 and MS are very small compared with M0, hence there is no considerable increase in the LNA’s input capacitance.

Simulated results: The linearity of both conventional and compensated LNAs is compared in Fig. 4. The linearity of the proposed LNA outperforms the linearity of the conventional LNA by more than 10 dB for input signal power as high as -14 dBm. Fig. 5 demonstrates the robustness of the compensation scheme; IIP3 figure improves by more than 9 dB for all technology corners. This plot also shows similar linearity figures for both architectures for input power signals greater than -5 dBm. For very large signals the compensating circuits enter into highly nonlinear regimes, mainly the transistor operating in the

subthreshold region MS. If huge input power is expected, operating points of both MT and MS have to be judiciously selected.

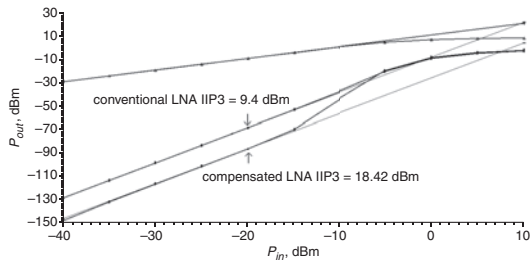


Fig. 4 Output power for both conventional and compensated LNAs at $T = 80^\circ$

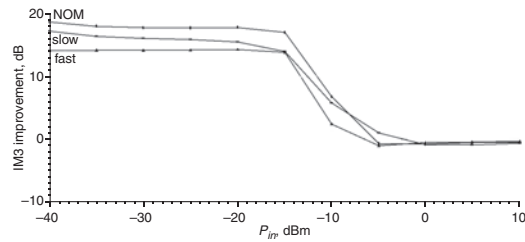


Fig. 5 IM3 improvement of compensated LNA over conventional one over three corners

Both topologies have been extensively simulated; the improvement of the proposed topology over the conventional LNA follows the trend of Fig. 5 for all technology corners and different temperature values. These results demonstrate that the proposed LNA healing technique is robust and effective under process and temperature variations. Additional results are provided in Table 1. Notice that the S12 and bandwidth for both topologies is similar because the compensating transistors MT, MS and M2 are small compared with M0. The extra power consumed by the additional circuitry is around 1 mW, that compared with the power dissipated by the main transistor represents an increment of around 5.5%. The noise figure decreases by around 0.1 dB because of slight increase in gm_{eff} .

Table 1: Comparison of compensated and conventional LNAs

Parameter	Conventional LNA	Compensated LNA
Gain (dB)	11.0	11.3
$f_{-3\text{ dB}}$ (MHz)	1.63–3900	1.62–3600
IIP3 (dBm)	9.7	18.4
Power (mWatt)	16.7	17.7
Noise figure (dB)	8.4	8.3

Conclusion: A robust and efficient compensation scheme to improve the linearity performance with little penalty in power consumption (<6%), frequency response and NF is proposed. Extensive simulation results show improvement of more than 10 dBm in IIP3 for signal power as high as -14 dBm. The proposed linearisation scheme is

robust against process variations and temperature gradients. Although tested in a conventional common-source LNA, the proposed approach can be used in many other topologies.

Acknowledgment: The authors thank Jazz-Semiconductor for providing access to their 0.18 μm CMOS technology.

© The Institution of Engineering and Technology 2009

4 November 2008

doi: 10.1049/el.2009.3168

H.M. Geddada, J.W. Park and J. Silva-Martinez (*Electrical and Computer Engineering Department, Analog and Mixed Signal Center, Texas A&M University, College Station, TX, USA*)

E-mail: ghsamohan@neo.tamu.edu

References

- 1 Chang, Y.C., Abidi, A.A., and Gaitan, M.: 'Large suspended inductors on silicon and their use in a 2- μm CMOS RF amplifier', *IEEE Electron Device Lett.*, 1993, **14**, pp. 246–248
- 2 Chehrazi, S., Mirzaei, A., Bagheri, R., and Abidi, A.A.: 'A 6.5 GHz wideband CMOS low noise amplifier for multi-band use'. Proc. IEEE Custom Integrated Circuits Conf., San Jose, CA, USA, September 2005, pp. 801–804
- 3 Zhan, J.-H.C., and Taylor, S.: 'A 5 GHz resistive-feedback CMOS LNA for low-cost multi-standard application'. IEEE ISSCC Tech. Dig., San Francisco, CA, USA, 2006, p. 200
- 4 Pedro, J.C., and Perez, J.: 'Design techniques for low in-band intermodulation distortion amplifiers', *Microw. J.*, 1994, pp. 94–104
- 5 Qu, G., and Parker, A.E.: 'Analysis of inter modulation nulling in HEMT's'. Optoelectronics and Microelectronic Materials and Devices Conf., Canberra, Australia, December 1996, pp. 227–230
- 6 Toole, B., Plett, C., and Cloutier, M.: 'RF circuit implications of moderate inversion enhanced linear region in MOSFETs', *IEEE Trans. Circuits Syst. I, Fundam. Theory Appl.*, 2004, **51**, (2), pp. 319–328
- 7 Aparin, V., Brown, G., and Larson, L.E.: 'Linearization of CMOS LNA's via optimum gate biasing'. IEEE Int. Circuits System Symp., Vancouver, BC, Canada, May 2004, Vol. IV, pp. 748–751
- 8 Kim, B., Ko, J.-S., and Lee, K.: 'A new linearisation technique for MOSFET RF amplifier using multiple gated transistors', *IEEE Microw. Guid. Wave Lett.*, 2000, **10**, (9), pp. 371–373
- 9 Kim, T.W., Kim, B., and Lee, K.: 'Highly linear receiver front-end adopting MOSFET transconductance linearisation by multiple gated transistors', *IEEE J. Solid-State Circuits*, 2004, **39**, (1), pp. 223–229
- 10 Ganesan, S., Sánchez-Sinencio, E., and Silva-Martinez, J.: 'A highly linear low noise amplifier', *IEEE Trans. Microw. Theory Tech.*, 2006, **54**, (12), pp. 4079–4085
- 11 Aparin, V., and Larson, L.E.: 'Modified derivative superposition method for linearizing FET low-noise amplifiers', *IEEE Trans. Microw. Theory Tech.*, 2005, **53**, (2), pp. 571–581
- 12 Perumana, B.G., Zhan, J.-H.C., Taylor, S., and Laskar, J.: 'A 12 mW, 7.5 GHz bandwidth, inductor less CMOS LNA for low-power, low-cost, multi-standard receivers'. Proc. IEEE RFIC Symp., Honolulu, HI, USA, 2007, p. 57
- 13 Tanaka, S., Behbahani, F., and Abidi, A.A.: 'A linearization technique for CMOS RF power amplifiers'. Symp. on VLSI Circuits, Dig. Tech. Pprs, Kyoto, Japan, 1997