

High-Resolution RF to Digital Converter for Next Generation Broadband Communication Systems

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I. Summary

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The goal of this project is the design and experimental verification of a high-performance mixer-less receiver prototype for multi-standard communication systems. The receiver will employ a linear broadband low-noise amplifier (LNA) and a programmable high-resolution bandpass Sigma-Delta Analog-to-Digital Converter ($\Sigma\Delta$ -ADC) to acquire a number of standards; the desired channel is selected by using a flexible frequency synthesizer. The architecture avoids the use of analog RF mixing operations and base-band analog processors. The anti-alias filtering usually required for analog-to-digital conversion is inherently present in the bandpass loop filter, eliminating strong filtering requirements saving both area and power consumption, and minimizing the effect of out-of-band interferers.

During the first 9 months of the project, the specifications for each individual block were obtained. The architecture has been simulated and spread of components has been evaluated. We expect to get access to the Taiwan Semiconductor Manufacturing Corporation (TSMC) 90nm CMOS technology this summer and tape out the first version of the RF ADC architecture no later than December 2009. In the mean time, the low-noise amplifier, frequency synthesizer and a 200 MHz ADC prototype with automatic calibration have been designed and fabricated in 180nm shuttles. These were the main activities during this period:

- The project goals are reviewed in section II. In the same section, the current status of the project is described. 7 graduate students were collaborating in this effort. One undergraduate student was indirectly involved in the project designing a low frequency sigma-delta ADC; he learned the ADC fundamentals and will start his MSc program in Fall 2009. His research will be directly linked to this project.
- We have been able to finish the study of the front-end and two new low-noise amplifiers have been developed. The performance of one of them has been experimentally verified while the second chip is currently under fabrication. Linearity figures have been improved over 10 dB when compared with the state of the art while other relevant parameters such as noise, power consumption and frequency response are competitive. Designed in TSMC and Jazz Semiconductor 0.18 μm CMOS technologies, these topologies cover the 1-5 GHz frequency band, but expect to extend their operation from 1-7 GHz when using the 90nm technology. Preliminary results are described in section III.
- Since the ADC will operate at the GHz frequency range, the generation of low-jitter clocks is a must. To achieve this goal, we are currently proposing to use a low-jitter LC-based oscillator as a base line, and using injection locking techniques we generate the required clocks with even better jitter performance than the original LC topology. A new injection locking technique has been developed and experimentally verified. A description of the frequency synthesizer topology is provided in section IV.
- The challenges involved in the design of the RF receiver are discussed in section V. The ADC architecture and design issues involved are also covered in that section. The components spread as

well as the issues related to the wide tuning range of filter and DAC coefficient parameters are discussed as well.

- As a proof of concept, we designed and tested a 200MHz $\Sigma\Delta$ -ADC prototype using a 0.18 μm CMOS technology thanks to the support of TSMC. The preliminary characterization of the 6th order ADC shows over 65dB signal to noise plus distortion ratio in 10MHz Bandwidth. We are currently improving the test setup and expect to achieve over 72 dB of SNDR. Design details are provided in section VI.
- In the same shuttle we included the automatic calibration technique based on the use of plurality of signals that measure the noise transfer function. The architecture will allow us to calibrate the ADC for the best possible performance using a software based algorithm. We are currently working on the testing set-up, and expect to have the experimental results in late June. The current status is further described in section VII.
- Finally, in section VIII we discuss the issues that will be addressed during the second year of the program.

Students involved in this project. We currently have 5 graduate students and 1 undergraduate student working on the different blocks. 4 PhD students will continue working on this project, 1 MSc will complete his work in August and probably will continue towards his PhD under the umbrella of this project, 1 undergraduate will continue collaborating in this effort as MSc student after graduation in May. 2 MSc students concluded their parts and graduated recently. We will incorporate another PhD student during the fall semester of 2009. The team is composed by the following students:

Cho-Ying Lu: PhD Senior student (International). Design leader of the 200MHz BP $\Sigma\Delta$ prototype, and system designer for the multi-standard receiver.

Chung-Yung Lo: PhD Junior student (International). Designer of the frequency synthesizer.

John Mincey: PhD Junior student (*Domestic*). Designer of the programmable loop filter.

Younghoon Song: PhD Junior student (International). Designer of the LNA, version I.

Mohan Geddada: MSc Senior student (International); will graduate in August 2009, and will pursue his PhD if we are able to raise funds to sponsor his program. Designer of the LNA, version II.

Alejandro Vera: Undergraduate student. (*Domestic, Hispanic*). He graduated on May and will start his MSc program in Fall-2009. For his senior project he designed a wireless glucose monitoring system employing a $\Sigma\Delta$ modulator based ADC.

The following students are co-designers of the 200MHz prototype:

Fabian Silva-Rivas: MSc student. (*Domestic, Hispanic*); graduated in May 2009. Fabian is currently with Broadcom Corporation. Design leader for both 2-bit quantizer and automatic calibration system for the 200MHz prototype. He also participated in the design of LNA version I.

Praveena Kode: MSc student. (International); graduated in January 2009. Praveena is currently with Nvidia Corporation. She designed the excess loop delay compensator for the 200MHz prototype.

Related papers reported during this period:

- [1] F. Silva-Rivas, C.Y. Lu, P. Kode, B. K. Thandri, and J. Silva-Martinez, "Digital Based Calibration Technique for Continuous-Time Bandpass Sigma-Delta Analog-to-Digital Converters," *Analog Integrated Circuits and Signal Processing*, Vol. 59, pp. 91-95, April 2009.
- [2] H. M. Geddada, J. Won-Park and J. Silva-Martinez "Robust Derivative superposition Method for Linearizing Broadband LNAs," *IEE Electronics Letters*, Vol. 45, pp. 435-436, April 2009.
- [3] Cho-Ying Lu, Fabian Silva-Rivas, Praveena Kode, and Jose Silva-Martinez, "A 200MHz CT Bandpass Sigma-Delta Modulator With Over 65dB-SNDR in 10MHz Bandwidth," submitted to the IEEE Custom International Circuits Conference, April 2009.
- [4] Yung-Chung Lo, Hsien-Pu Chen, Jose Silva-Martinez and Sebastian Hoyos, "A 1.8V, Sub-mW, Over 100% Locking Range, Divide-by-3 and 7 Complementary-Injection-Locked 4 GHz Frequency Divider," submitted to the IEEE Custom International Circuits Conference, April 2009.

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