Task Title: A Hybrid 14-bit Analog-to-Digital Converter for Broadband Applications

Funding: Awarded

Task Leader: Prof. Jose Silva-Martinez

Principal Investigator: Prof. Jose Silva-Martinez

Co-Principal Investigator: Prof. Aydin Ilker Karsilayan

ITRS Grand Challenge:

3. High-Performance, Low-Cost RF and Analog/Mixed-Signal Solutions (Radio Frequency and Analog/Mixed Signal Technologies for Wireless Communications)

NEEDS -TEXAS ANALOG CENTER OF EXCELLENCE

C2.1 Robust continuous time sigma delta ADCs for wide bandwidth radio applications

Primary Anticipated Result (50 words max)

To develop techniques for the design of vanilla CMOS low-voltage low-power high-resolution continuous-time analog-to-digital converters with full on-chip digitally-based calibration system. The techniques will be compatible with emerging nanometer technologies.

Task Background (200 words max)

Broadband connections with different wireless networks require high-resolution analog-to-digital conversion solutions, especially when weak target signals are hidden within a background of strong interferers. Direct conversion transceivers with soft filtering in front of the ADC and the huge out of band power due to high frequency blockers demand very high resolution ADCs. Industrial interest in finding efficient solutions becomes evident when revising the recently announced GRC ITRS grand challenges and the efforts reported by SRC members.

The focus of this proposal is to develop efficient design techniques, fabricate and test a low-voltage low-power broadband high-resolution continuous-time analog-to-digital converter that can be exported to deep-submicron CMOS technologies. The proposed architecture will be able

to provide an outstanding figure of merit in the range of 250 pJ/conversion-step since it makes extensive use of digital based quantizer and DACs that are tolerant to clock jitter. Three major tasks have been identified:

i) Develop and verify the operation of high-performance continuous-time data converter architecture suitable for low-voltage nanometer technologies.

ii) Develop design strategies for low-voltage low-power building blocks for baseband applications

iii) Develop an intensive-digital on-chip calibration methodology for ADC signal-to quantization-noise ratio optimization.

Task Deliverables for transfer to industry *(30 words each max)*

i) Participate in annual research reviews
ii) Provide annual reports and pre-defined deliverables as follows:

July 2010:

- Documentation of the top level core architecture and description of the behavioral simulation results. (preliminary report will be available on December 2009)
- Technical report describing the design aspects of critical building blocks including schematic simulation results. (preliminary report will be available on May 2010)
- Technical report describing the floor plan of the layout, and post-layout simulations (July 2010)

July 2011:

- Description of the testing set-up and a report describing the experimental results of the first chip (preliminary report will be available on December 2010)
- Technical report describing the schematics of the second chip that includes the complete fully-calibrated architecture (July 2011)

July 2012

- Technical report describing the floor plan of the layout, and post-layout simulations. (preliminary report will be available on December 2011)
- Final report describing the testing set-up and experimental results for the fully calibrated 14-bit resolution ADC. Report will include final conclusions and will suggest future directions (July 2010)

Graduate Students:

To be decided