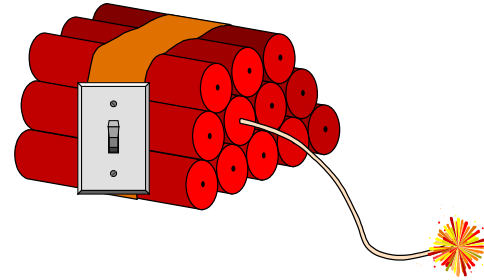


Analog and Mixed-Signal Center



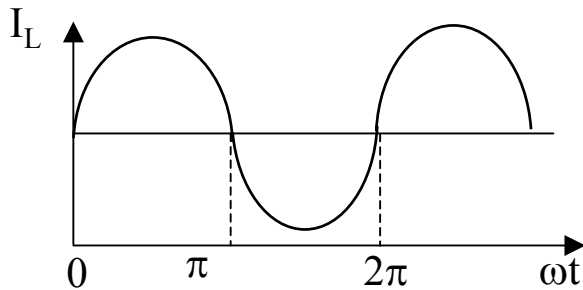
Power Amplifiers

Edgar Sánchez-Sinencio

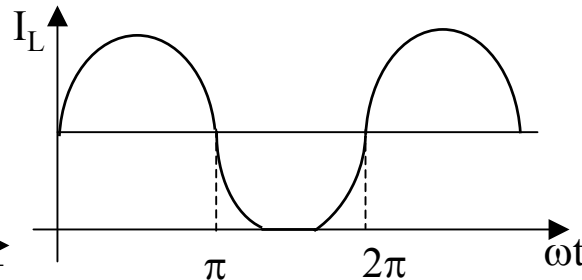
**Analog and Mixed-Signal Center, Texas A&M University
Department of Electrical Engineering**

POWER AMPLIFIER CLASSES

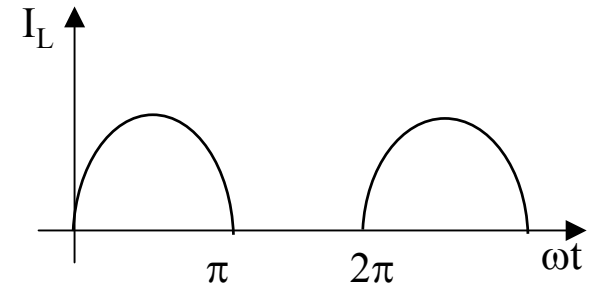
- Class A consumes large power even for no AC input
- Class A consumes power all the time



Maximum efficiency 25%
Class A



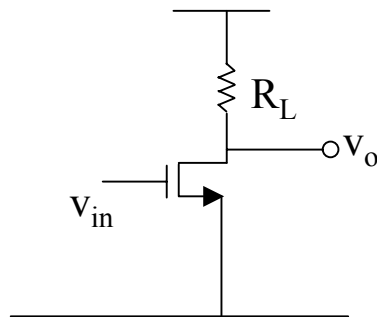
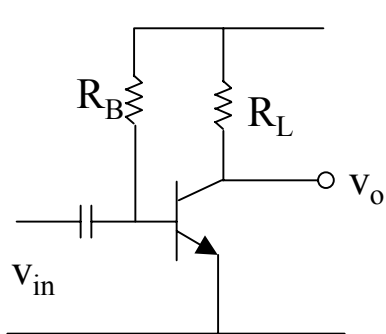
Class AB



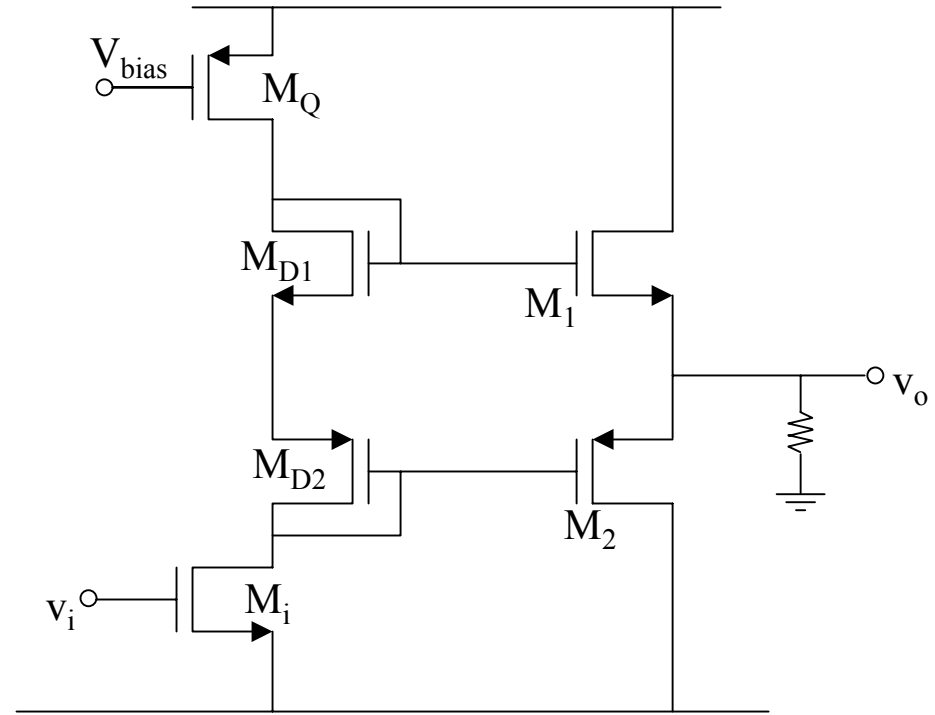
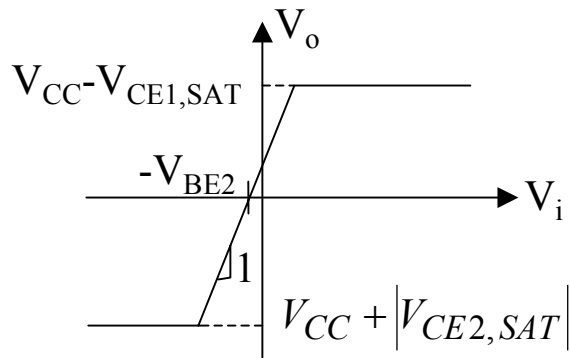
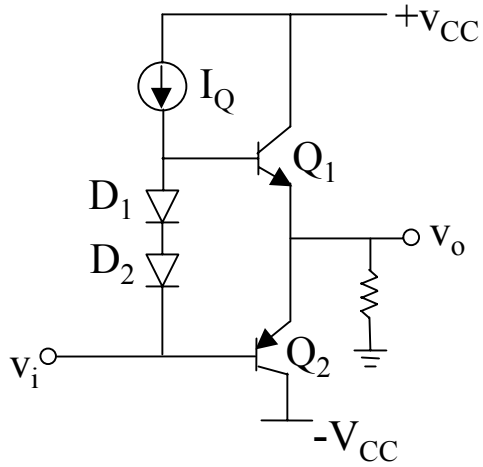
Maximum efficient 78.5%
Class B

Power Amplifiers classified based on the load current

How to use other than Class A and still have low distortion?
Can a single transistor amplifier be distortion less?



CLASS B OUTPUT STAGE CIRCUITS



- This circuit can not handle 20mA

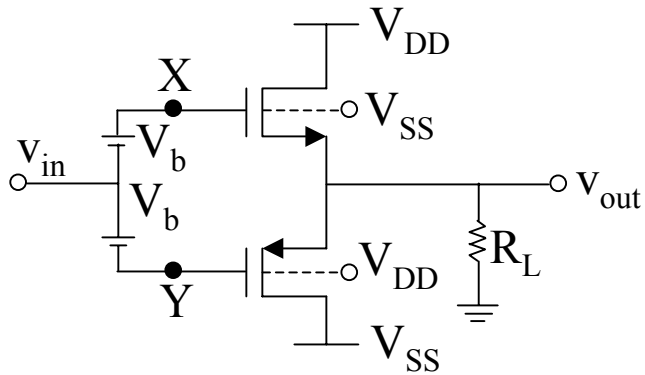
$$\frac{W}{L} \bigg| = \frac{2I_D L}{K_p W (V_{GS} - V_T)} \bigg| = 25,000 \quad \text{☹}$$

$$K_p = 40 \mu A / V^2$$

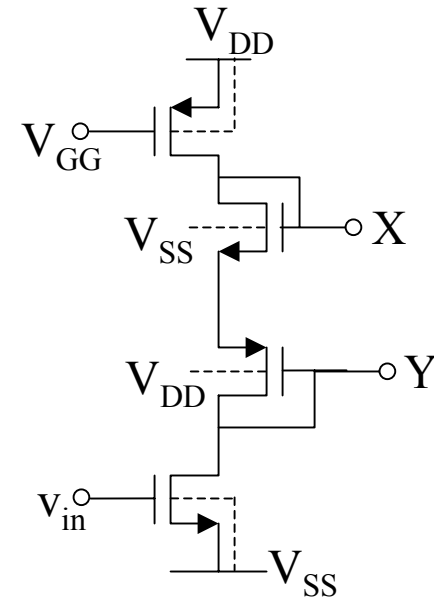
$$V_{GS} - V_T = 0.2$$

$$I_D = 20 mA$$

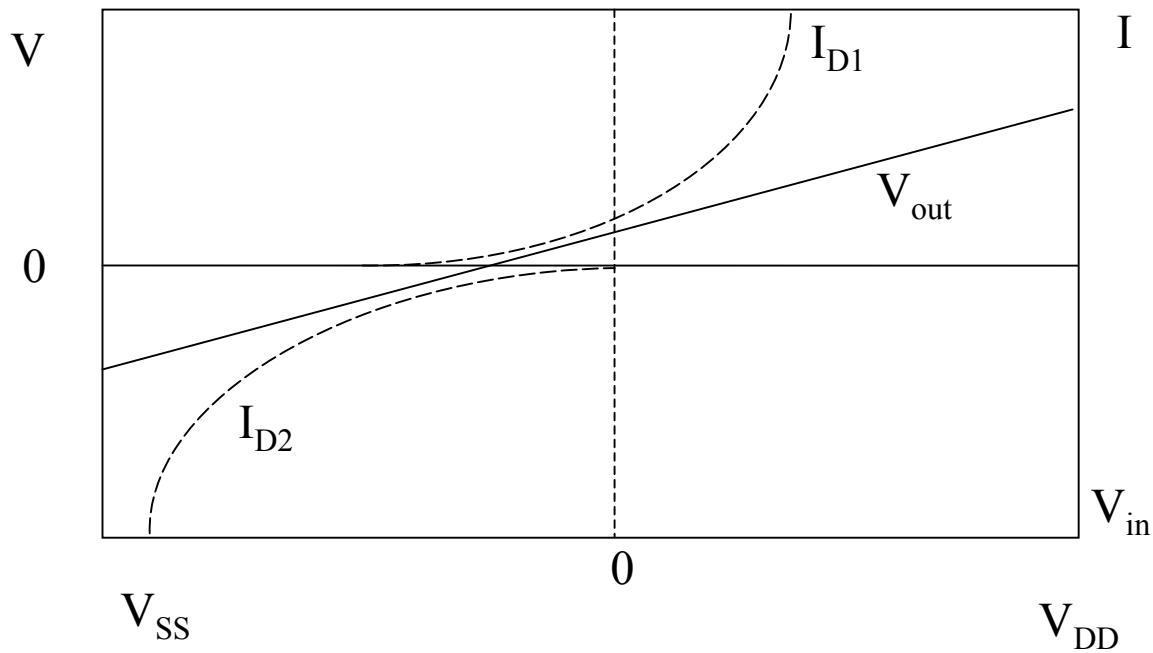
CLASS AB AMPLIFIERS



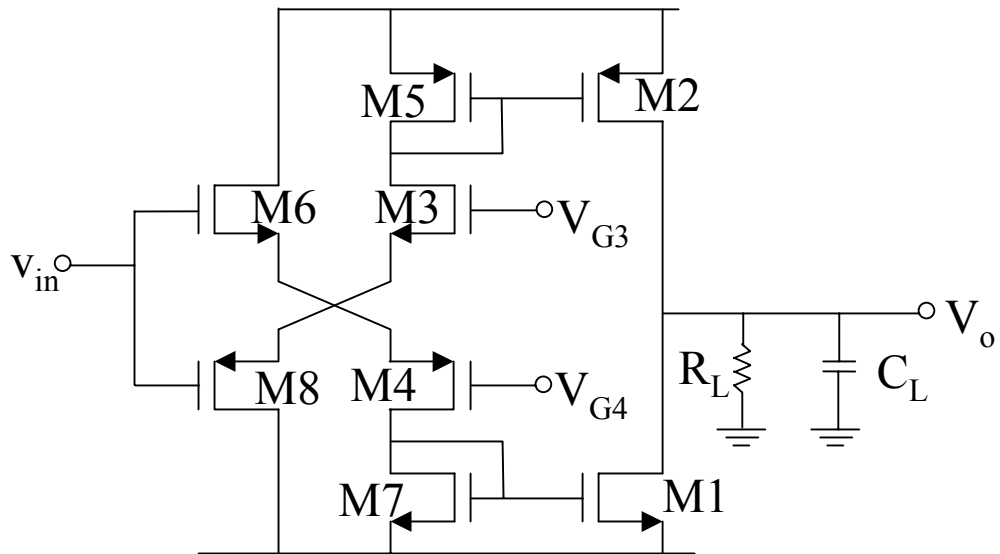
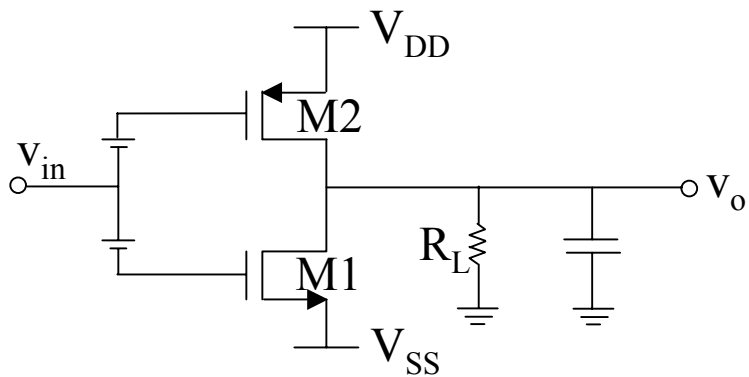
Push-Pull Source Follower



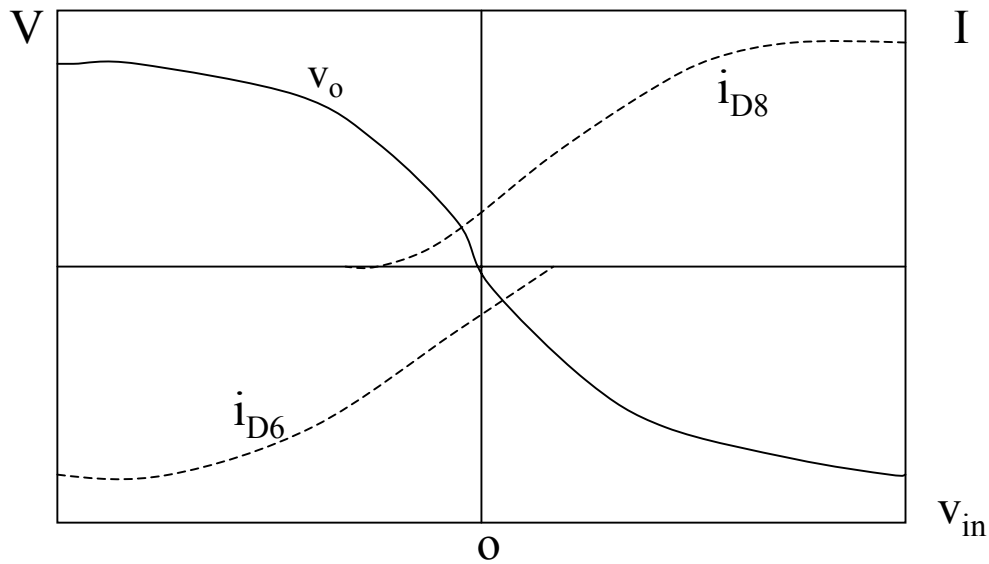
V_b (Floating Batteries) Implementation

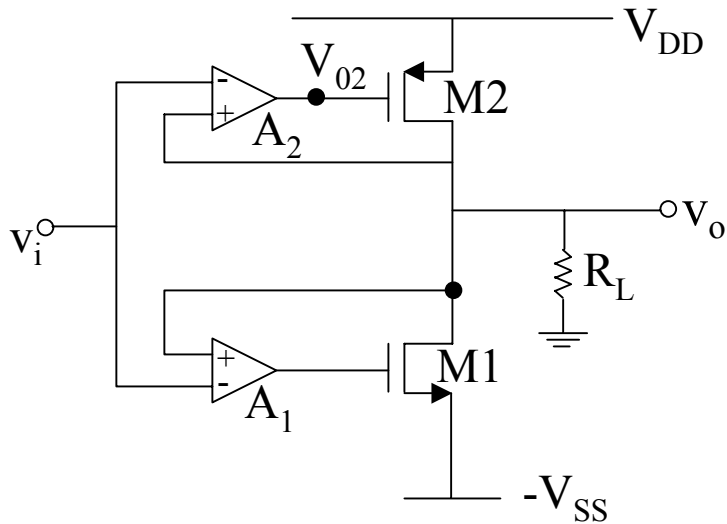


PUSH-PULL INVERTING AMPLIFIER



$$V_{in} \uparrow + \quad I_{D6} \uparrow \quad I_{D8} \downarrow \quad I_{D1} \uparrow$$





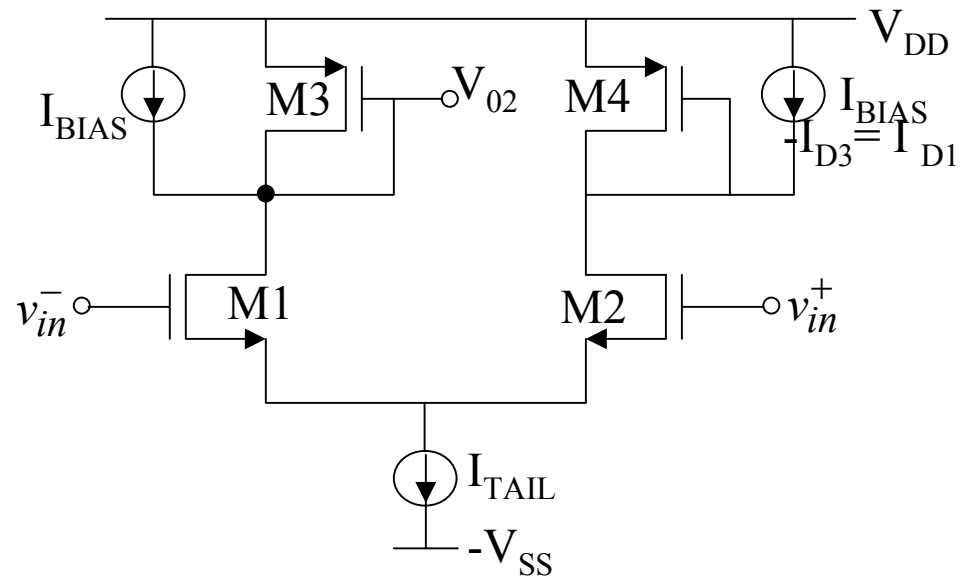
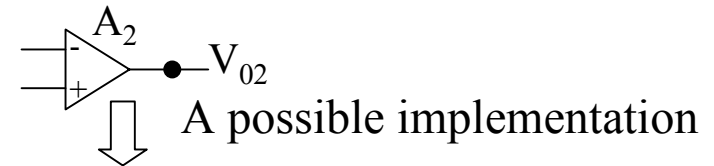
Class B using enhanced common-source output stage.

$$A_v = \sqrt{\frac{K'_n(W/L_1)}{K'_p(W/L)} \frac{I_{D1}}{I_{D1} - I_{BIAS}}}$$

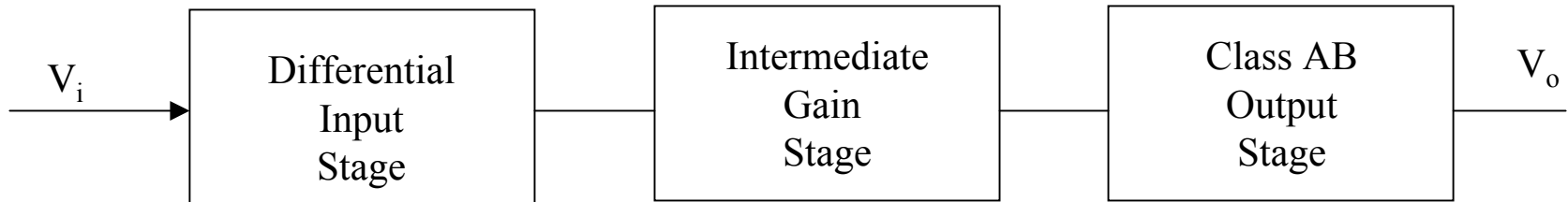
Note that

$$\frac{I_{D1}}{|I_{D3}|} = \frac{I_{D1}}{I_{D1} - I_{BIAS}}$$

- M1 and M2 can produce output voltage that approach the power supply voltage.
- A_1 , A_2 must be broadband to prevent crossover distortion.
- Problems handling large C_L .



CLASS AB AMPLIFIERS

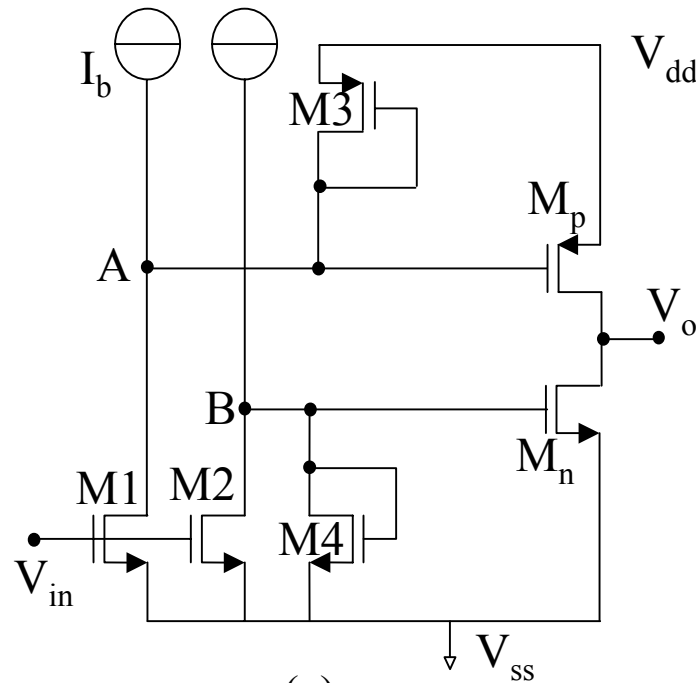


Typical Op Amp Structure

Class AB

- High Power Conversion Efficiency
- Current handling capabilities to drive small resistive loads
- Push-Pull solutions are not suitable for low voltage conditions.
- I_Q (idle conditions) must be small

Principle of Class AB with Adaptive Load



(a)

- Low gain of intermediate stages (M1-M3), (M2-M4) 😊
- Limited V_{GS} swing at Mn and Mp ☹️

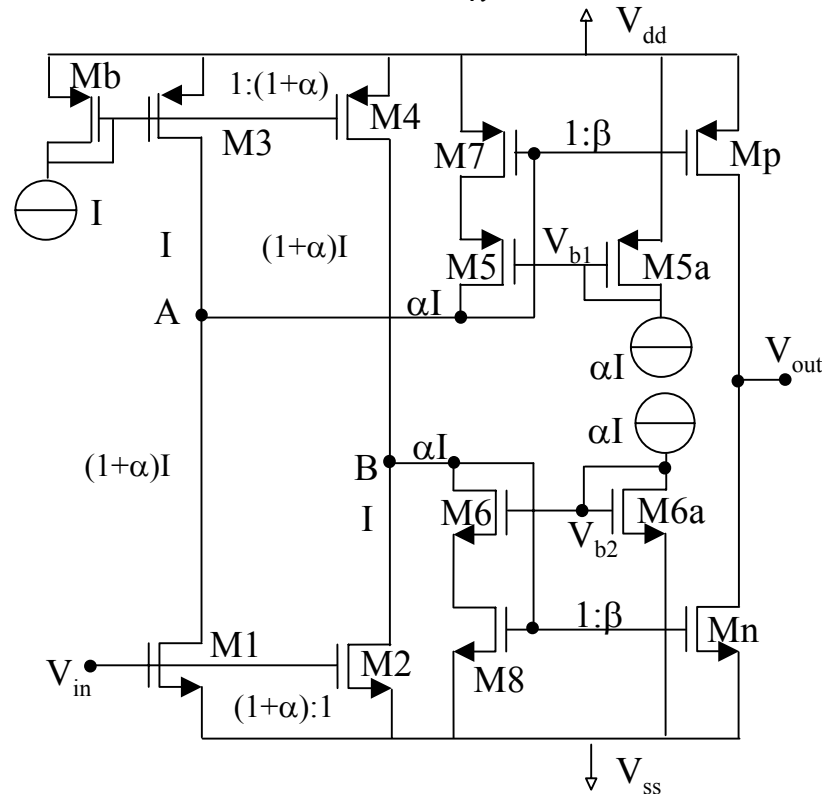
How to tackle this problem?

⇒ Use an adaptive load at nodes A and B

- Under I_Q (idle) conditions the load should be small to make I_Q less sensitive to Process mismatch
- In class B mode

$v_{in} \uparrow R_A \uparrow V_A \uparrow$ maximum drive for M_p

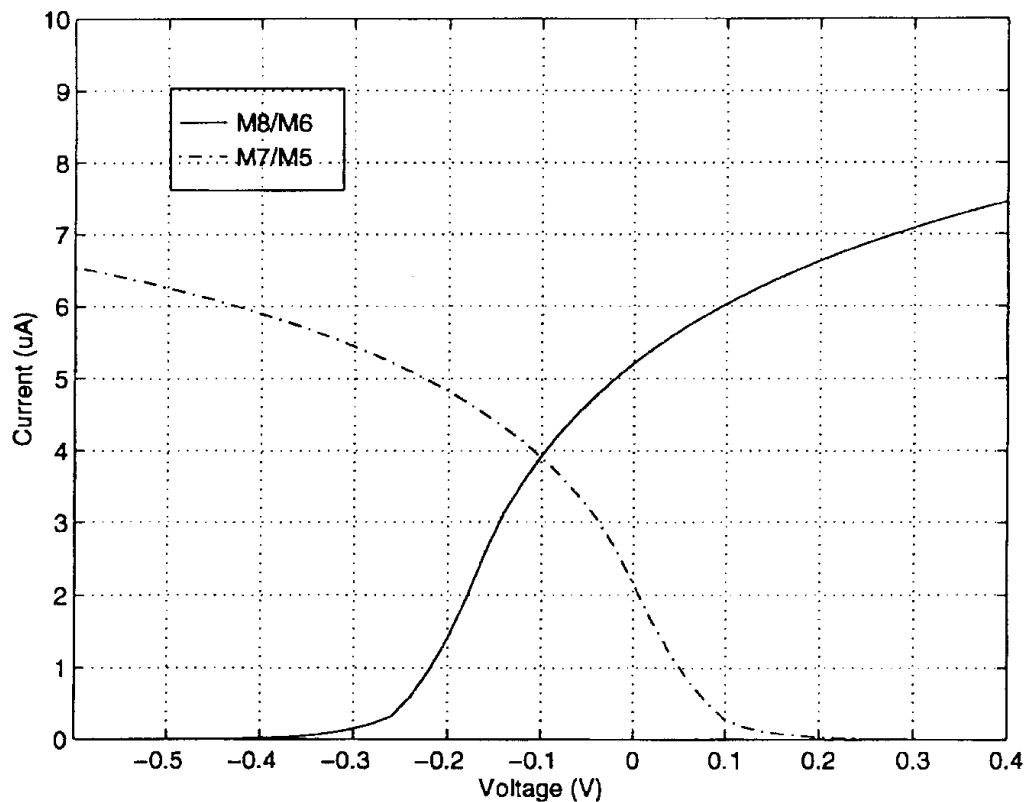
$v_{in} \downarrow R_B \uparrow V_B \uparrow$ maximum drive for M_n



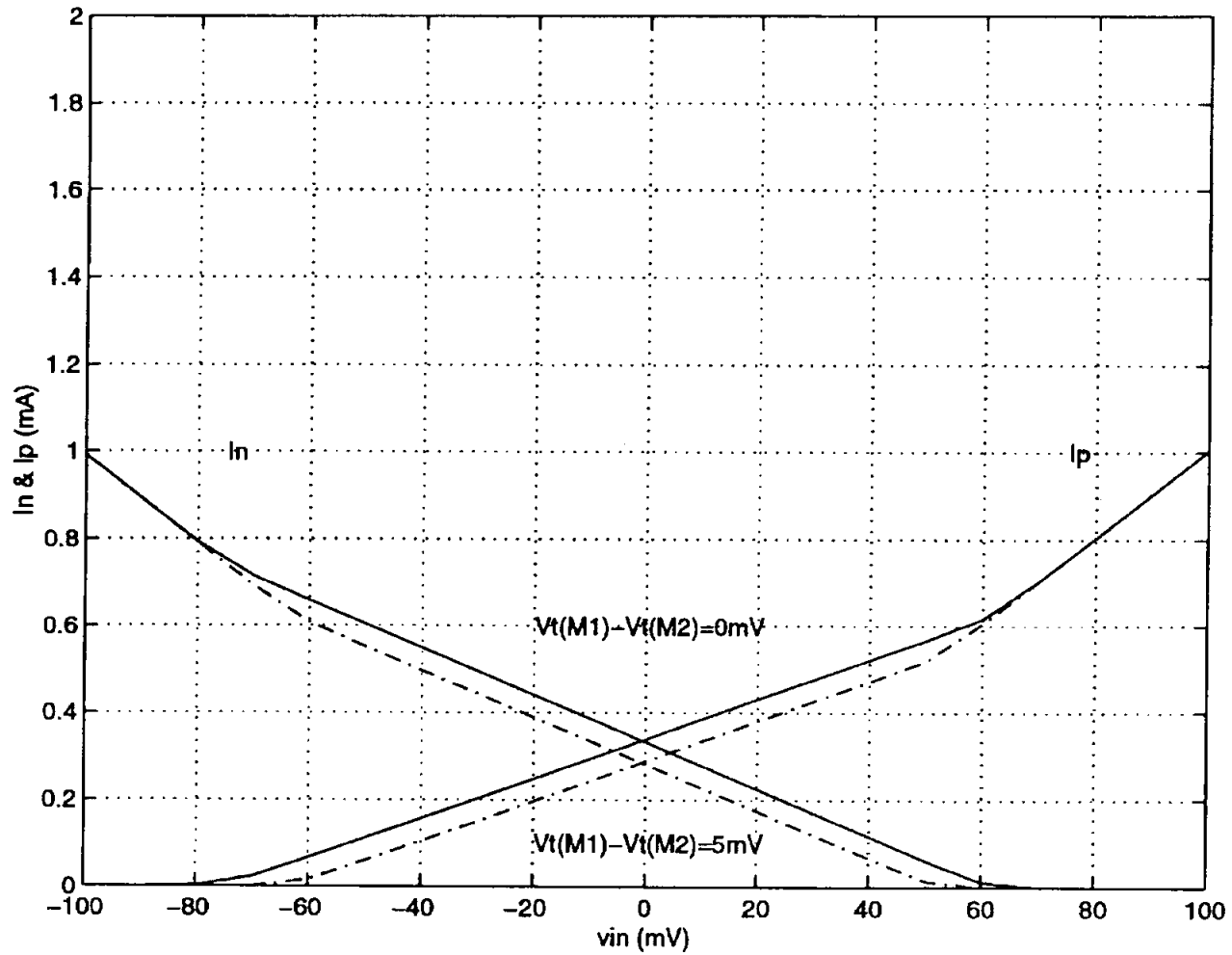
(b) Output buffer with adaptive load

- M_6/M_8 and M_5/M_{17} Adaptive loads

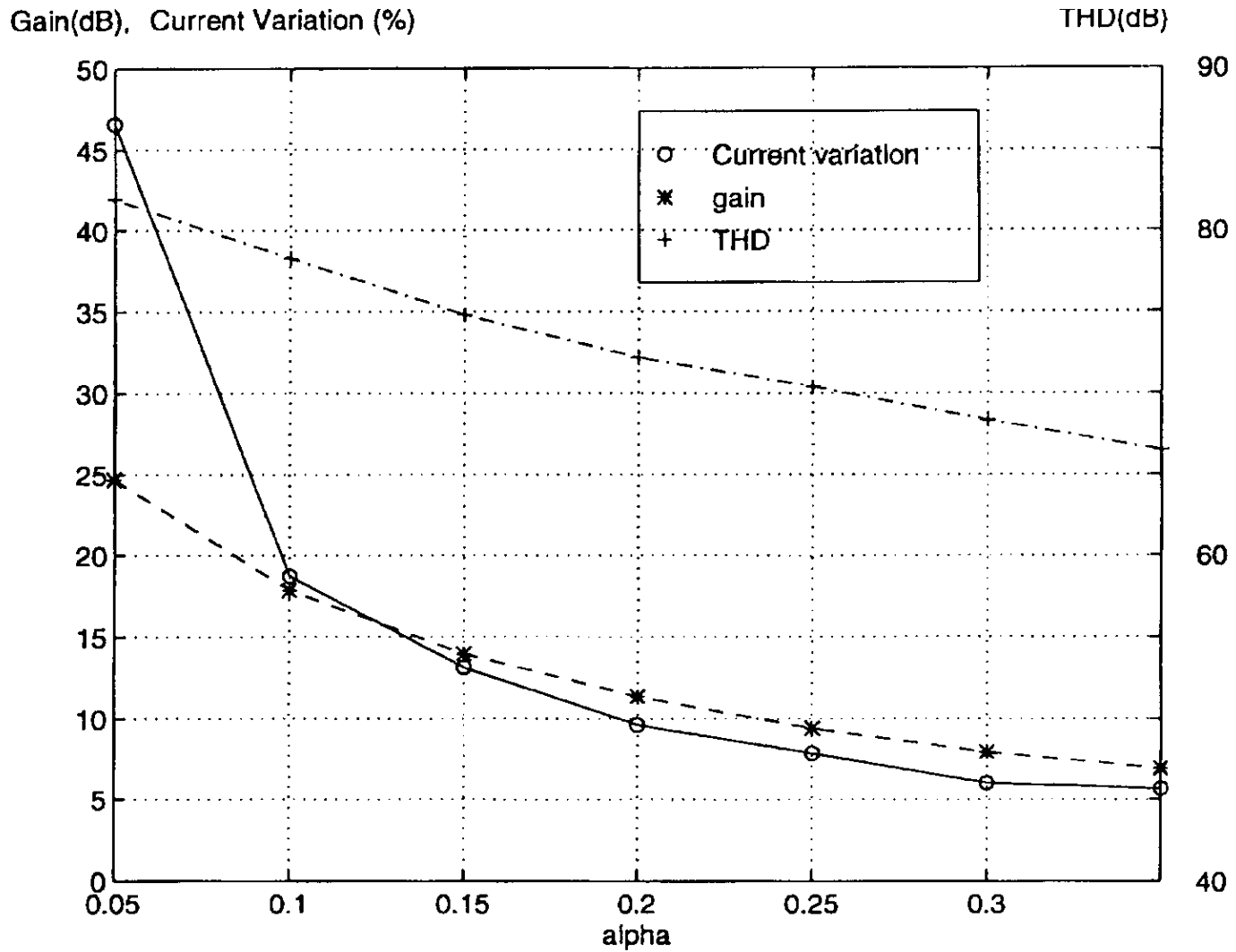
| Transistors | Quiescent Conditions | Class B Mode |
|--|--------------------------|--|
| M ₅ (M ₆) M ₇ (M ₈) | Saturation Saturation | Out of saturation Out of saturation |
| Loading at A(B) | SMALL | LARGE |



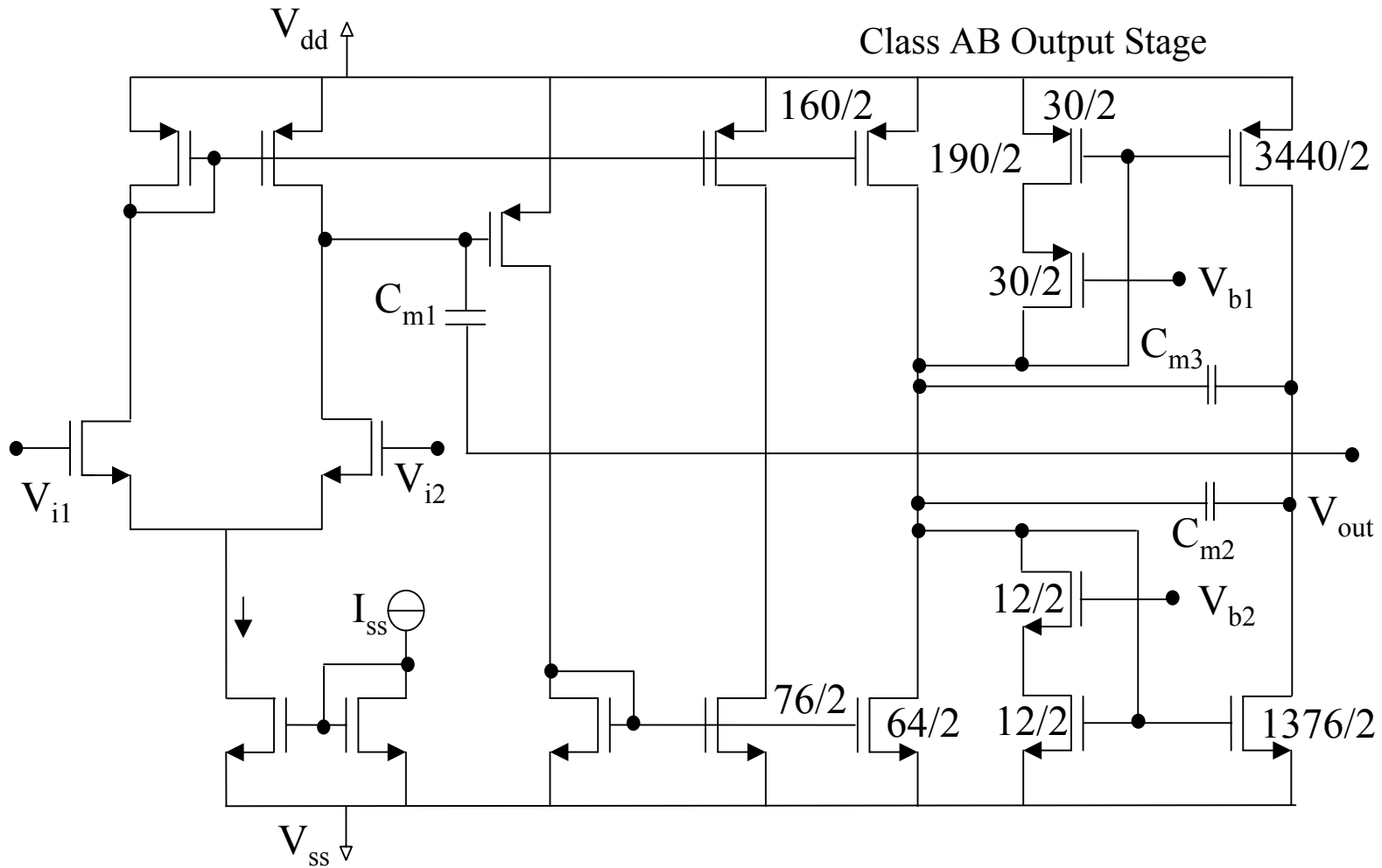
Simulated I-V characteristics of the adaptive loads in Fig. 1(b) (X axis is V_{in})



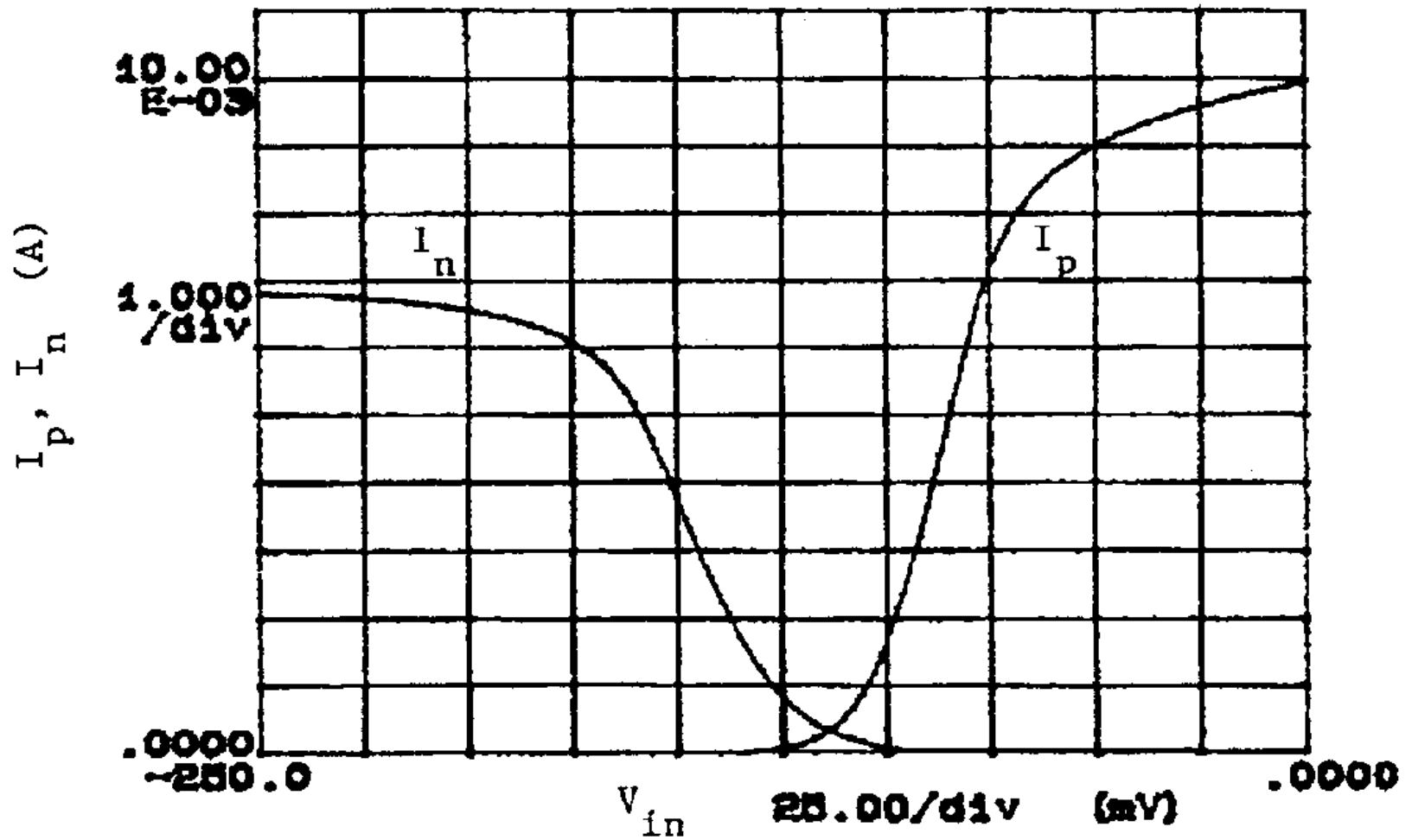
Simulated variation of the quiescent current with and without 5 mV V_T mismatch.



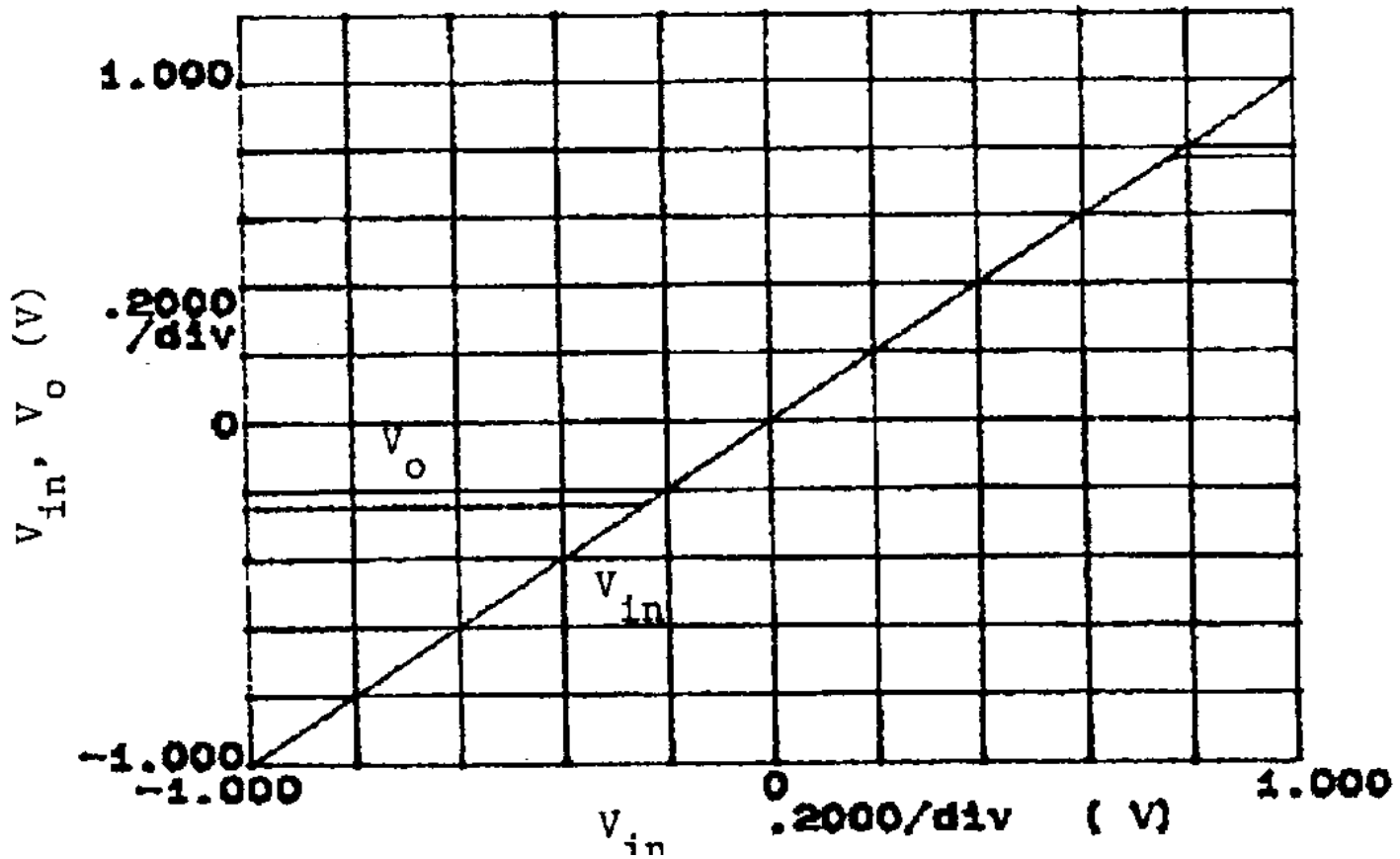
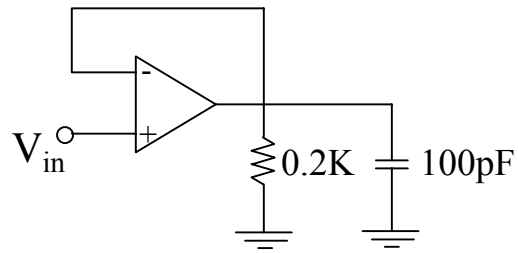
Simulated quiescent current, voltage gain at node A, and the THD as a function of α .



Schematics of the low-voltage op amp used to test the output buffers.
CMOS 2.0 μ m technology.

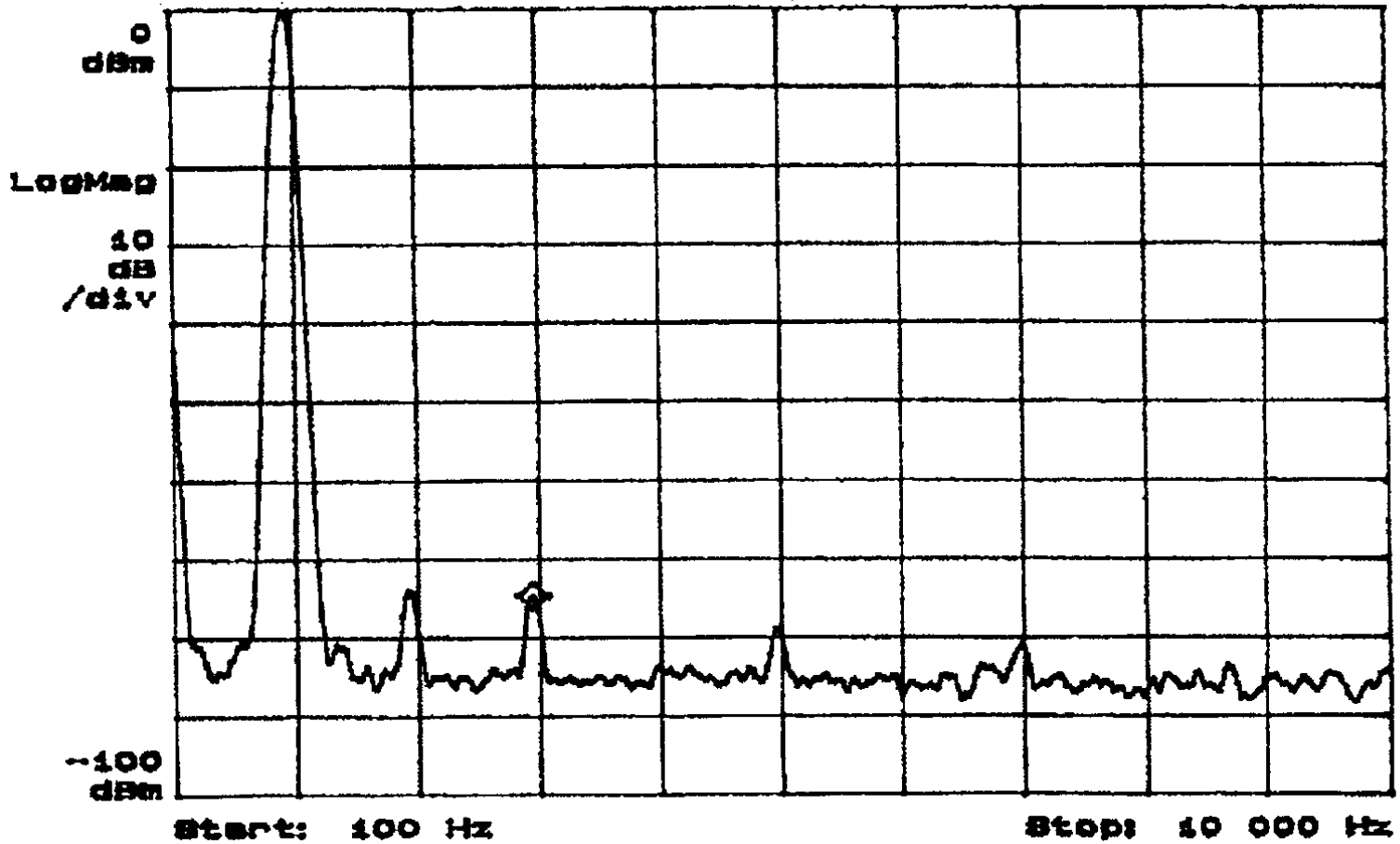


Measured output current of the class AB output buffer.
 $I_Q \cong 272 \mu A$ Variations do not affect performance.



Measured output voltage versus input voltage of the unity-gain follower.

$$V_T = 0.86V$$



Magnitude spectrum at the output node of a unity-gain follower with 1 kHz sine wave input. Power supply 2V.

...they are actually lighting one another) but a smoother transfer of the workload from one

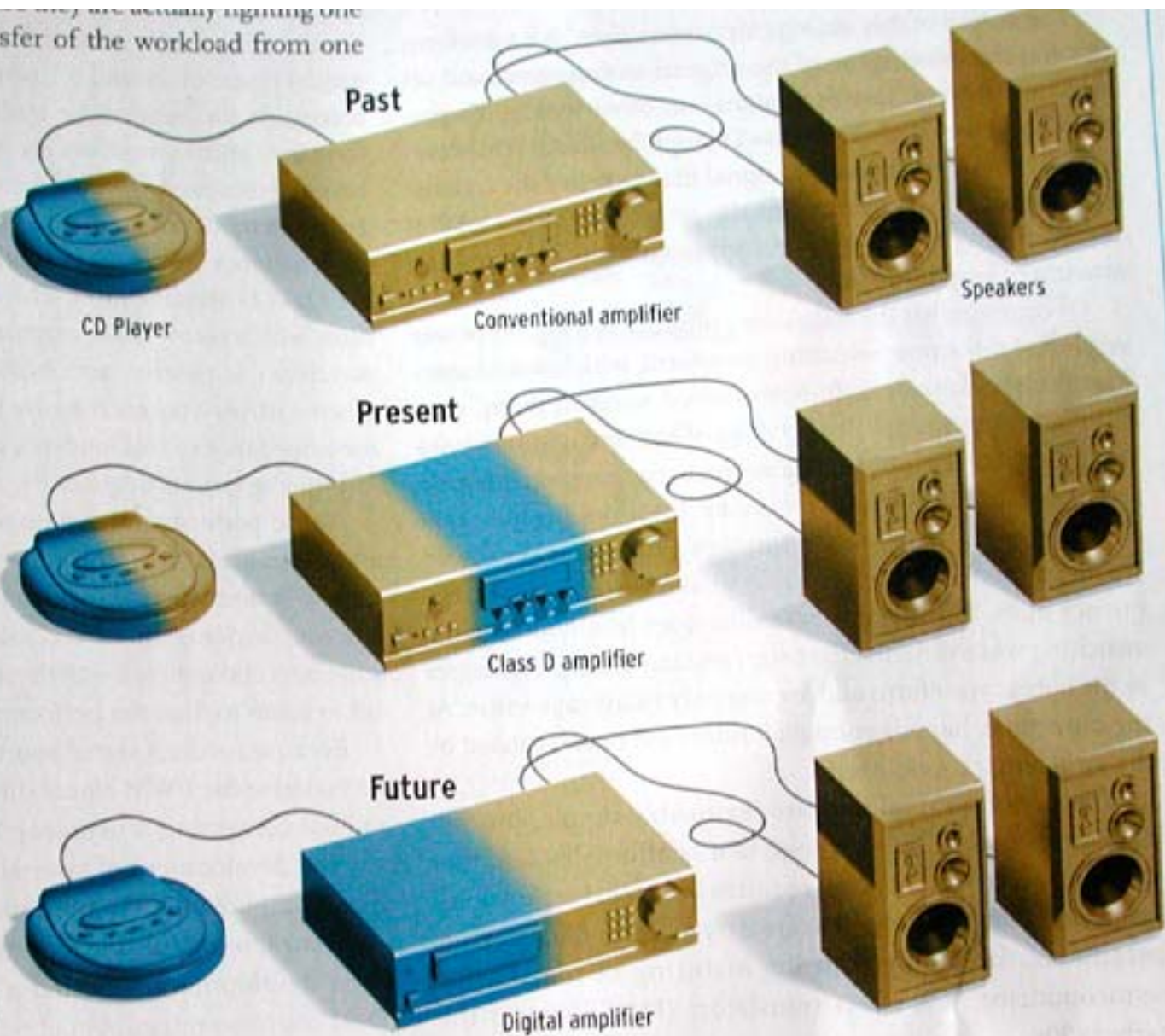
■ Digital
■ Analog

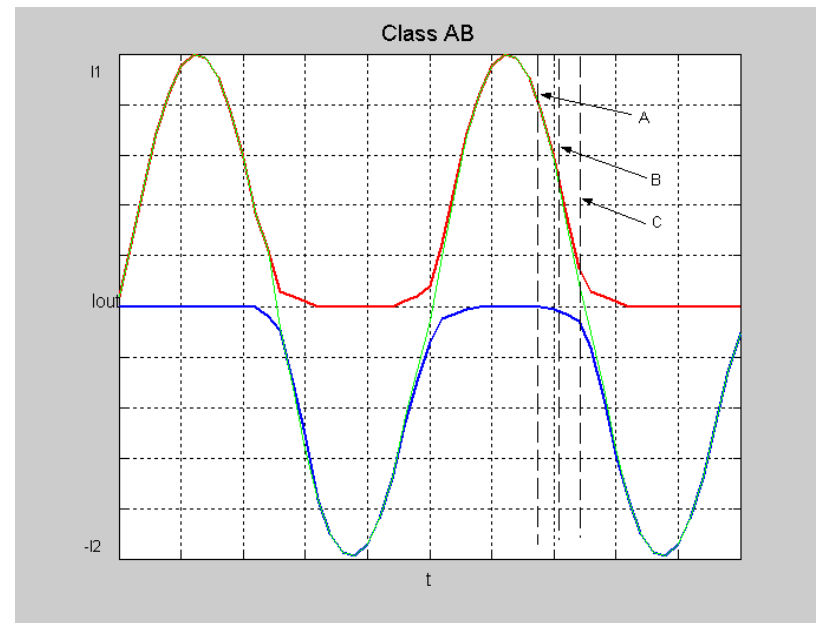
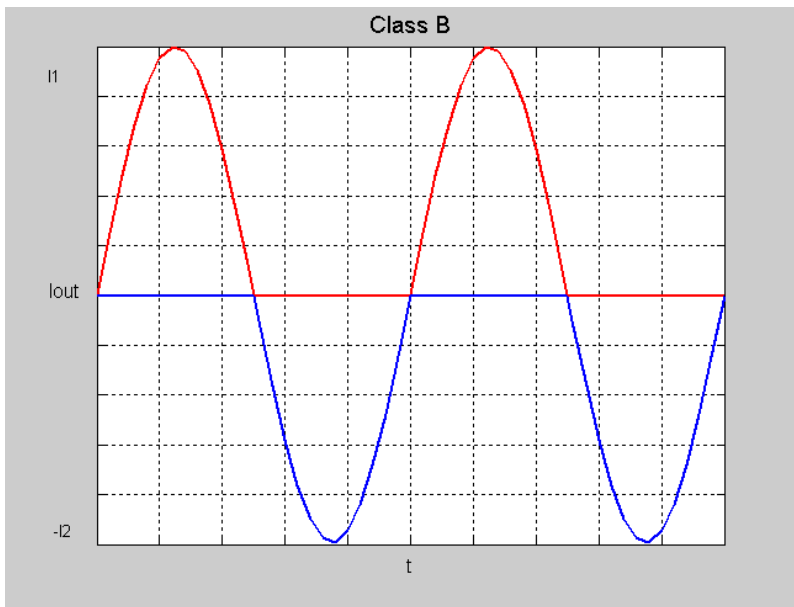
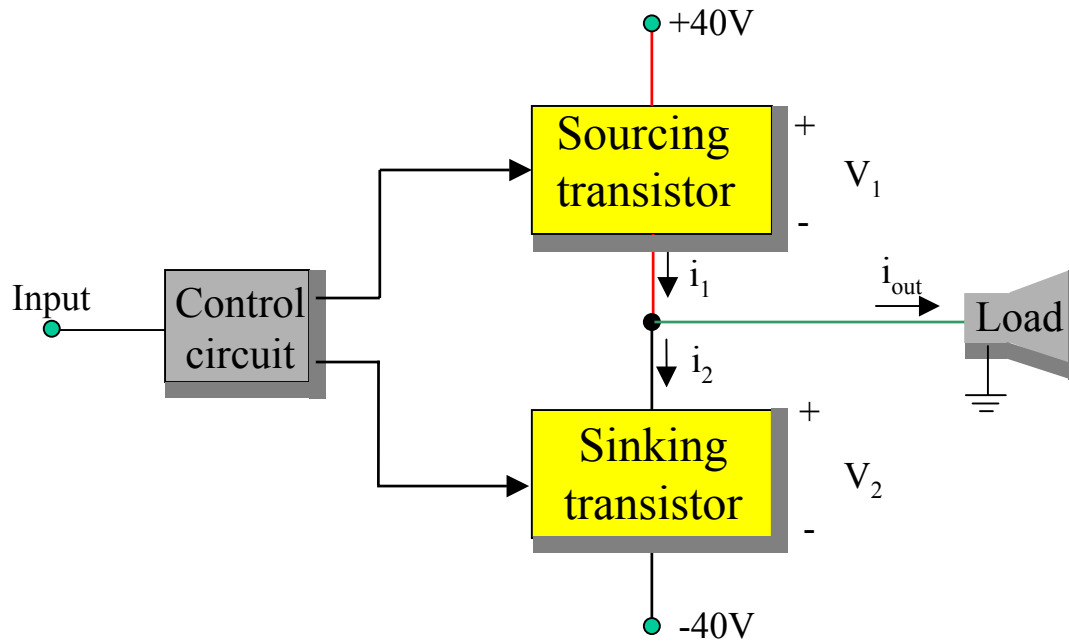
Yesterday, Today, & Tomorrow

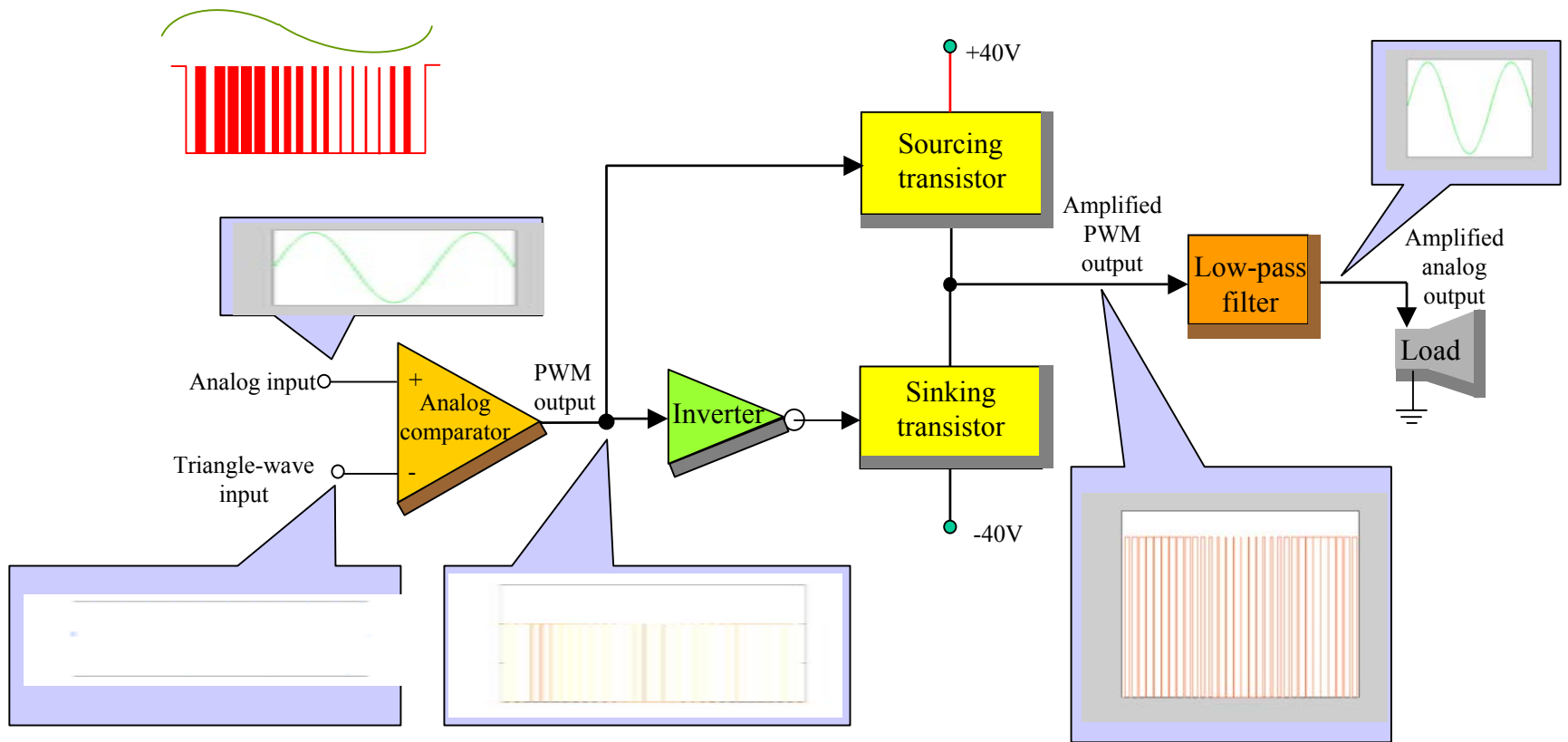
Yesterday, a CD player would be partly digital [blue] and partly analog [gold]. It would send analog signals to all-analog amplifiers [top].

Today's latest amps are partly binary. They accept analog inputs, amplify them by switching, and put out analog signals [center].

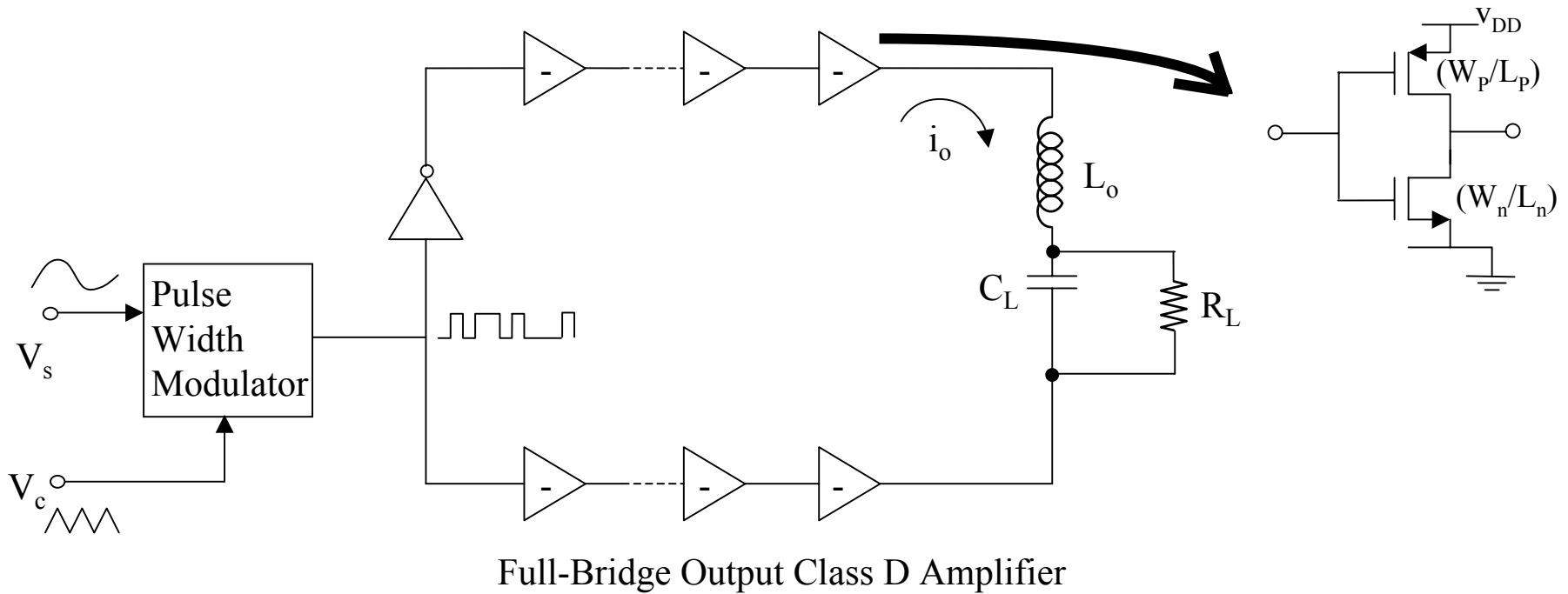
In the future, digital sources will feed digital amps, again converting to analog only at the output [bottom].







CLASS D AMPLIFIER OUTPUT STAGES



Power Dissipation Mechanisms:

$$P_c = f_c C_p V_{DD}^2 / 2$$

Parasitic Capacitance

$$P_s = I_{mean} V_{DD}$$

Short - Circuit current
During Transitions

$$P_r = \frac{1}{T_s} \int_0^{T_s} i_o^2 r_{on} dt$$

On - Resistance

OPTIMIZATION TO A SINGLE MODULATION INDEX

$$\text{Power efficiency} = \eta(W_p) = \frac{1}{1 + F(W_p)}$$

where $\eta = P_{out}/P_E$, P_E is the total power drawn from the supply.

$$F(W_p) = \frac{P_c + P_s + P_r}{P_{out}}$$

$$\frac{\partial F(W_p)}{\partial W_p} = 0 \quad \text{Yields Max } \eta(W_p)$$

Assume $L_n = L_p = \min L$, $K'_p = K'_n$, then

$$W_p = D \sqrt{\frac{B_1}{B_1 + B_2}} \quad , \quad W_n = W_p / \alpha$$

Where D is the modulation index (V_s/V_c) , V_s is the peak voltage of the input signal, and V_c is the peak Voltage of the triangular carrier signal. B_1 , B_2 are layout dependent, see table for details.*

* J. S. Chang, H-T Tan, Z. Cheng, and Y-C. Tong, "Analysis and Design of Power Efficient Class D Amplifier Output Stage,"

IEEE TCAS-I, Vol 47, No. 6, pp 897-902, June 2000.

- The higher D the better η at the cost of area

How about the case of variable D?

$$\eta(W_p, D) = \frac{P_{out}}{P_{out} + P_c + P_s + P_r}$$

$$= \frac{X_1 D^2}{X_2 D^2 + X_3}$$

where

$$X_1 = I_o^2 R_L / 2 \quad , \quad X_2 = I_o^2 (r_{on} + R_L) / 2 \quad , \quad X_3 = P_c + P_s$$

For a range of D, $\Delta D = D_2 - D_1$ the average power efficiency is

$$\eta_{av}(W_p) = \frac{1}{\Delta D} \int_{D_1}^{D_2} \eta(W_p, D) dD$$

$$\eta_{av}(W_p) = \frac{1}{\Delta D} \left\{ X_4 D_2 - X_4 \sqrt{X_5} \tan^{-1}(D_2 / X_5) - X_4 D_1 + X_4 \sqrt{X_5} \tan^{-1}(D_1 / X_5) \right\}$$

Where

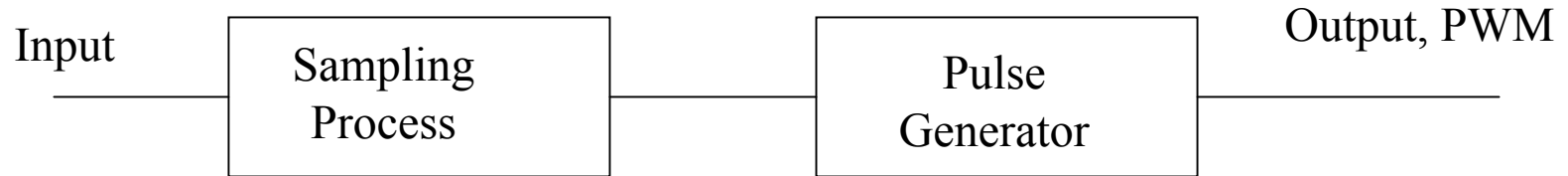
$$X_4 = \frac{X_1}{X_2} \quad , \quad X_5 = \frac{X_3}{X_2}$$

$$\frac{d\eta_{av}(W_p)}{dW_p} = 0 \quad \text{Does not yield a closed expression. A numerical solution is needed.}$$

The remaining transistor widths of the preceding stages are designed according to the tapering factor T.

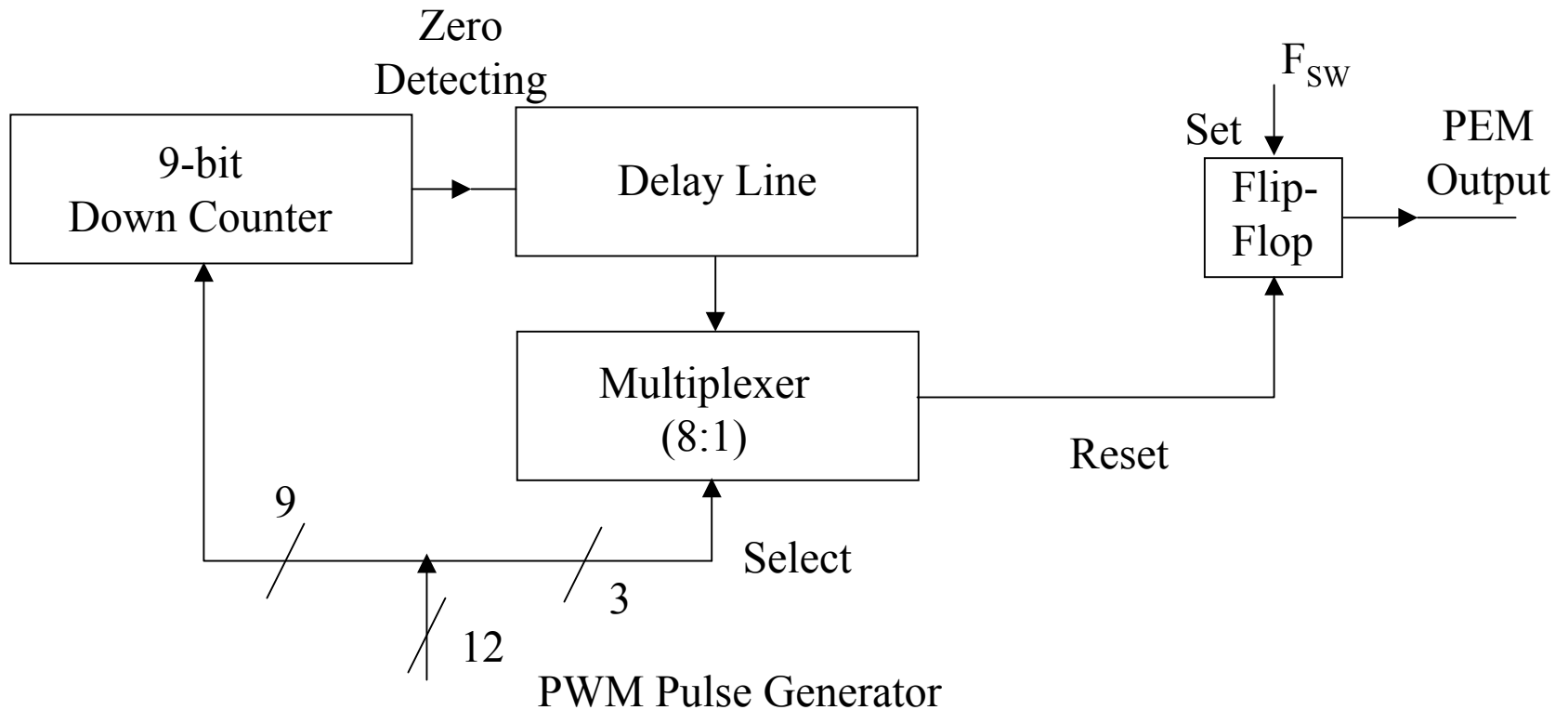
Observe that the huge size of W_p (thousands of μm) require finger or waffle layouts.

- A digital class D amplifier involves a digital pulse width modulation (PWM), output stage and a low pass filter.
- PWM comprises the stages



- The output stage is a cascade of inverters whose transistors have increasing aspect ratios, and the final stage has low output impedance.
- The low pass filter removes the carrier components, thus yielding a continuous-time output signal.

- PWM* Pulse Signal
- Fast Clock Counter
 - Tapped - Delay Line Based \rightarrow DLL needed.
 - Combination of counter - delay - line based.



* H. Li, B.H. Gwee, and J.S. Chang, "A Digital Class D Amplifier Design Embodying a Novel Sampling Process and Pulse Generator," *Proc. ISCAS*, IV-826 – IV-829, 2001.