ELEN 607 (ESS) Spring ‘08

PROPOSED FINAL PROJECTS

These final projects can be done by one student, or a team of two or three students. The level of work and innovation should be proportional to the number of students. Please provide a hard copy of a list of your three preferred projects by April 1st . All projects will use AMI 0.5µm unless it is specified otherwise..

Project 1. *Bandgap reference voltage.* Design a high PSR CMOS based bandgap reference voltage using the 0.5µm technology with the following specifications:

Bandgap output Voltage = 1.2V
Power supply range = 2V to 3.3V
Current Consumption = 80µA
PSR: -100@1KHz, -65@1MHz
Temperature Drift = 3mV for the temperature range -40^{o} to 125^{o}

Compare at least two techniques for achieving the required high PSR. In some practical applications, the designer adds an RC filtering stage at the output (off chip capacitor) of the bandgap. Does this technique help to reduce the power consumption? What should be the corner frequency of the filter? Propose a modification in the existing architecture to either reduce the power consumption or enhancing the PSR at 1MHz.
It is important during the design phase to check the stability of the bandgap using transient simulations and ensure a phase margin of 60^{o}. Check the operation of the bandgap around the corners of the technology.

- K.-M. Tham and K. Nagaraj, “A Low Supply Voltage High PSRR Voltage Reference in CMOS Process,” Journal of solid state circuits, vol. 30, pp.586-590, May1995
- S. Hoon, J. Chen, and F.Maloberti, “An improved bandgap reference with high power supply rejection,” in International Symposium on Circuits and Systems, 2002.

Project 2. *High PSRR Amplifier*. Design a differential amplifier with high power supply rejection ratio that meets the following specifications:

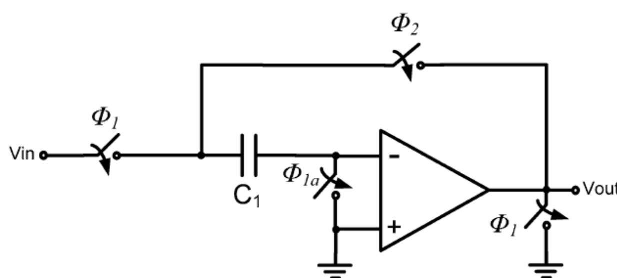
Voltage Gain = 60dB
GBW= 100MHz
Power supply range = 2V to 3.3V
Current Consumption = 25µA
PSRR: -90dB@1KHz, -70dB@1MHz, -45@10MHz

Compare at least two techniques for achieving the required high PSRR. The biasing circuit affects PSRR. Include the complete biasing circuit during your simulations. Assume that you have a single reference current of 1µA.
Propose a modification in the existing architecture to increase the power supply rejection ratio over a wide frequency range. Compare the proposed approach with the existing technique highlighting the power consumption, and variations across the process corners. In the final report provide a detailed analysis of the PSRR for the used architectures.

Ref.

- D.B. Ribmer and M.A. Copeland, " Design Techniques for Cascoded CMOS Op Amps with improved PSRR and Common-Mode Input Range," IEEE J. Solid State Circuits, vol SC-19, No. 6, pp919- December 1984
- J. Fisher, " A High Performance CMOS Power Amplifier", IEEE JSSC, vol SC-20, pp. 1200-1205, December 1985.

Project 3. Propose a rapid power-on Opamp for high speed pipeline ADC applications. Your OTA is to be used in a flip-around track-and-hold configuration as shown below (You should implement a differential version). Compare the transient response, SNDR & average power consumption for the T/H stage in two modes: 1) Opamp is on both at sampling and hold phase. 2) Opamp is only power on during hold phase, and is power off at sampling phase.

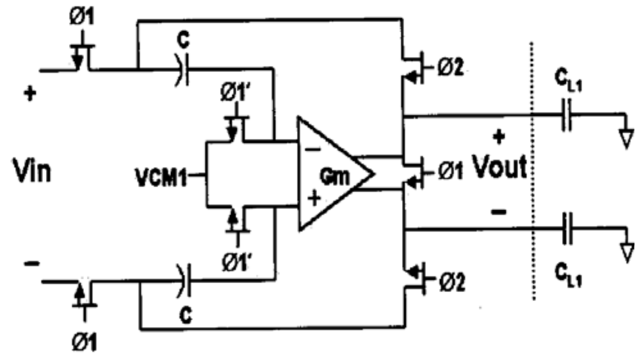


Specifications:
Vin: 2Vpp differential
Sampling rate: 80MSPS
Power: <70mW
SNDR: > 60dB
Power supply: 3V
Process: 0.35µm CMOS
the capacitors should be >0.5pF
Discuss the pros & cons of possible OTA topologies for this requirement and justify your choice. Explore the maximum sampling rate (beyond 80MSPS) you can achieve with mode 2 while maintaining SNDR > 60dB.

Reference:

[1] Imran Ahmed, and David A. Johns, "A 50-MS/s (35 mW) to 1-kS/s (15 µW) Power Scaleable 10-bit Pipelined ADC Using Rapid Power-On Opamps and Minimal Bias Current Variation", *JSSC Dec. 2005*

Project 4. Design an OTA for power scalable pipeline ADCs. The bias current of the OTA should be made dependent on the sampling rate, i.e., when the sampling rate increases, the bias current becomes larger, resulting in larger GBW and shorter settling time for the OTA. The OTA needs to be robust and maintain a constant DC gain against variation in bias current, with all transistors remain in saturation. Your OTA is to be used in a flip-around track-and-hold configuration as shown below.



Specifications:
Vin: 2Vpp differential
Sampling rate: 4MSPS~80MSPS
Power: 10mW~ 80mW
SNDR: > 60dB for all sampling rate
Power supply: 3V
Process: 0.35µm CMOS
the capacitors should be >0.5pF
Discuss the pros & cons of possible OTA topologies for this requirement and justify your choice. Propose a scheme to make the biasing current changes automatically with the clock rate.

Reference:
[1] K. Gulati and H. S. Lee, "A low-power reconfigurable analog-to-digital converter," *IEEE J. Solid-State Circuits*, vol. 36, no. 11, pp. 1900–1911, Dec. 2001.
[2] Govert Geelen, Edward Paulus, Dobson Simanjuntak, Hein Pastoor and Rene Verlinden, "A 90nm CMOS 1.2V 10b Power and Speed Programmable Pipelined ADC with 0.5pJ/Conversion-Step", *ISSCC 2006*

Project 5. . Design a capacitorless LDO using approaches not employed in HW# 8, the specifications to meet are:

V_{OUT}/V_{DROP}	1.6V-2.0V/200-400mV
$I_{MAX, LOAD}$	10mA
$I_{MIN, LOAD}$	0.01mA
C_{OUT}	100pF-1000pF
Δ V_{OUT} (Full Load)	<90m@C_L=100pF
Settling	<16µA (0-50mA)
Quiescent Current	Not counting the current load <50µA
PSR (1KHz)	<-60dB
Noise @ 10^5Hz	$< 0.7\mu V/\sqrt{Hz}$

Operating temperature range is from -40C to +85C. Discuss alternatives of using NMOS pass transistors without using charge pump. Provide at least two versions.

Project 6. Design a fully differential constant-g_m rail-to-rail Op Amp that meets the following specifications:

Load	1MΩ//15pF	50Ω//33pF
DC Gain (dB)	>180	>140
GB (MHz)	> 60	> 35
Phase Margin (deg)	> 62	> 72
Average Slew Rate (V/µs)	> 55	> 42
CMRR (dB)	≥110	≥100
V_{out} Swing	rail-to-rail	rail-to-rail
Power Consumption (mW)	<15	<16
Power Supply	± 1.35V	

Project 7. Design a fully differential 1 volt CMOS amplifier using bulk driven and/or floating gate techniques, and negative resistors. The specifications are

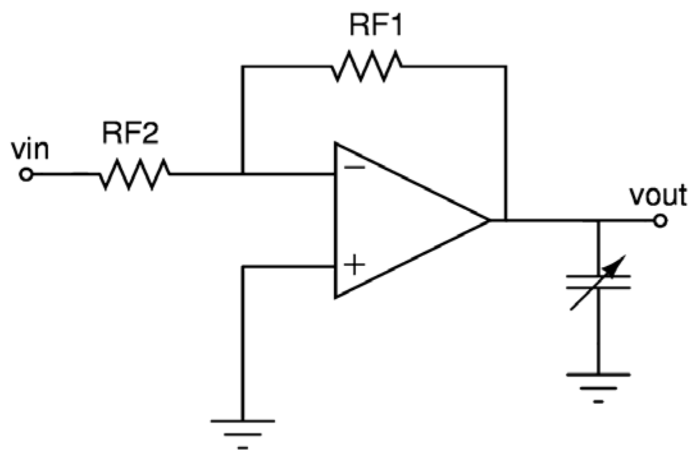
GB	≥ 100 MHz
A_o	≥ 120 dB
Acl	5 (non-inverting configuration using resistors)
Load	0.5pF-1.0pF// 20K
V_o	close to rail-to-rail
Power Supply	1V or ± 0.5V

Discuss also techniques to improve PSRR, settling time and CMRR.

Project 8. Amplifier for LDO Applications. Design an amplifier using 0.5um CMOS technology with the following specifications:

A_o > 60dB
GBW > 2MHz
Phase Margin > 60°
PSRR > 65dB @ 1MHz
Power Supply = 3.5V
Load Capacitance varies from 20pF to 80pF
Current Consumption < 20µA
Input Common Mode Voltage =1.2V
Settling Time < 100ns

Verify the stability and transient response of the amplifier using the following configuration:



Where, RF1 and RF2 are 420KΩ and 240 KΩ, respectively. Use an input step of 3.3V to verify the settling time. Can you achieve a settling time smaller than 90ns? If not, propose a technique to improve the settling time. In addition, estimate and simulate the PSR and propose a technique to improve it.

Project 9. Design a Class-D Amplifier using Delta-Sigma based or another technique not based on triangular wave reference. Meet or improve the specs described in the last row (This work) of the following table.

CLASS D AUDIO AMPLIFIERS COMPARISON

Design	THD	η	Supply	Load	I_0	FOM
[3]+	0.20%	-	3.0 V	8 Ω	-	-
[4]	0.28%	92%	2.5 V	8 Ω	25.2 μA	1.3
[5]+	0.50%	85%	-	-	-	-
[6]+	0.11%	70%	5.0 V	8 Ω	-	-
[7]	0.03%	76%	4.2 V	8 Ω	4.7 mA	5.4
[8]+	0.20%	90%	5.0 V	4 Ω	-	-
[9]*	0.08%	85%	5.0 V	4 Ω	8.0 mA	1.3
[10]*	0.40%	87%	2.7 V	4 Ω	2.8 mA	0.8
[11]	0.04%	79%	3.6 V	8 Ω	2.5 mA	7.9
[12]+	0.10%	92%	12 V	8 Ω	-	-
This work	0.08%	91%	2.7 V	8 Ω	2.0 mA	5.7

* Commercial product.
\+ Not full data reported.

Ref.- *Miguel Rojas-Gonzalez, and E. Sánchez-Sinencio, "Design of a Class D Audio Amplifier IC Using Sliding Mode Control and Negative Feedback" IEEE Transactions on Consumer Electronics, vol. 53, no. 2, pp. 609-617, May. 2007.*

The important dates are:

Progress Report (April 17, 2008) with discussion of the specifications; clearly define the problem, preliminary simulations and identification of the future work and a summary of the reported related publications in the literature. No more than 6 pages. This report is worth 10% of the final project. This (word document) report **must** have the following form:

Title
Statement of the problem.
Background, previous work.
Potential applications of your circuit. You must provide specific examples and references.
Basic idea of your solution. Preliminary Results.
Problems to be solved in the near future.
References, a complete list of references must be included.

Final Written Report (May 1, 2008). This final (word document) report must include:

1. Title
2. An abstract
3. Introduction
4. Background and a comparative table of previous results
5. Proposed Solution
   - Conceptual idea of solution
   - Circuit Diagram and explanation
   - Design Procedure, how to determine the (W/L)'s
   - The temperature, noise and process variation effects
6. A Comparative Table between Hand calculation and Simulation
7. Discussion of Results with other reported results and suggested improvements
8. Layout of the Circuit
9. References

Oral Presentations in Power Point Form: April 22, 23, 24 (if needed), 2008.