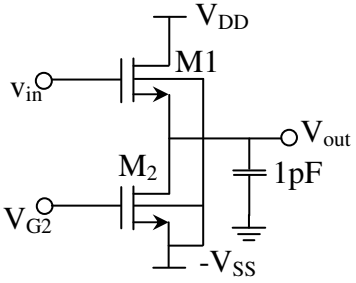
**ELEN 607 (ESS)** **Due: January 24, 2008**
**SPRING '08**

# HOMEWORK ASSIGNMENT #1

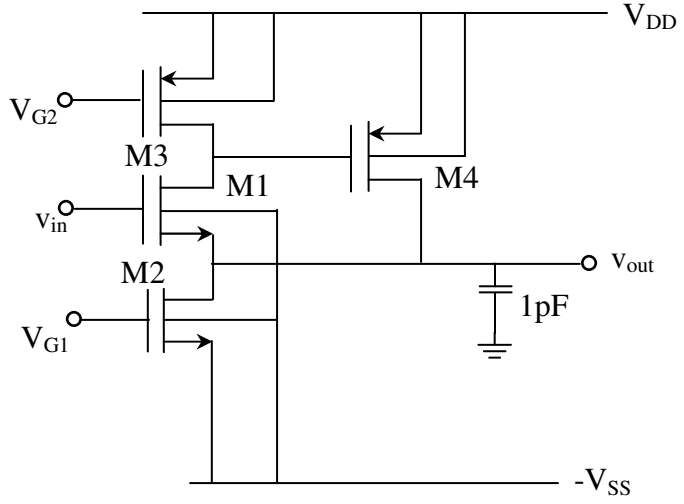
Prob. 1. Use any size technology and generate the equivalent plot (see page 21 Lect. #1) of various parameters versus the inversion level. i.e. $f_{T,}$ power consumption, (W/L) vs $i_f$. Also in another graph plot $f_{max}$ vs $i_f$ for at least two different W/L families, i.e. (W/L) = (100µ/0.6µ, 100µ/3µ). Make comments.

Prob. 2. Extract the parameters ofs transistor PMOS and NMOS for the ACM model, that is one equation all regions. See Ref. 6 on Lect. #1. Consider the 0.5µm CMOS technology and $i_f$ = 8. Discuss how the parameters are extracted. Provide a table summarizing results of the extracted parameters. Discuss results.

Prob. 3 Design two low impedance buffer using the circuits shown below. Use $i_f$ = 8 and 0.5µm CMOS technology, $V_{DD}$ = -$V_{SS}$ = 1.65V. Provide design procedures.




Buffer 1




Buffer 2

Include a summarizing table with at least, Max $v_{out}$ , Max $I_{out}$, voltage gain, output impedance, $f_{3dB}$, $PSRR^+$, $PSRR^-$, settling time 0.1%, power consumption, $C_{in}$, input referred noise, CMRR and CMR. Discuss how they compare.