

HOMEWORK # 2

Prob. 1. A non-inverting amplifier with 3.3 V/V closed loop voltage gain with minimum input capacitance is required. Therefore, design a two stage Op Amp using 0.5 μ m technology. Use the all region-one equation transistor model. Provide the design for 3 splitting techniques i) RC type, ii) source follower and iii) capacitor with current buffer*. The specifications to satisfy are:

A_{v_o} (DC)	>60dB
GBW	>195MHz
In-band noise (DC-50MHz)	<15 μ V
Phase Margin	>50 $^\circ$
Slew Rate	>160V/ μ s
Settling Time	<100ns
C_L	8pF
R_L	10K Ω
Power dissipation	<15mW
C_{in}	<1.5pF
R_{out}	<100 Ω @ 195MHz

Also use process parameter from the last three runs posted by MOSIS, indicate the difference (in%) from the last run. Provide this table.

Parameter	Run 1	Run 2	Run 3
Offset Voltage			
CMR			
Voltage DC Gain			
f_{3dB}			
Power consumption			
Input referred noise			

Provide, in addition, complete table(s) summarizing your result, for the last run. Show the step responses. Besides the specifications given above include PSRR, CMRR vs. f, power consumption, CMR range, maximum and minimum output voltages. *Discuss your results from Tables and simulation graphs.*

* See for instance R. Mita et al, “Design Guidelines for Reversed Nested Miller Compensation in Three-Stage Amplifiers,” *IEEE Trans. on Circuits and Systems II*, Vol. 50, pp. 227-233, May 2003.

Prob. 2. From Prob. 1, plot the open loop phase margin versus C_L , i.e. {0.1 – 100}pF. Now propose how can you modify your amplifier topology to keep it stable under large range of the capacitive load C_L . *Show that your approach works.*

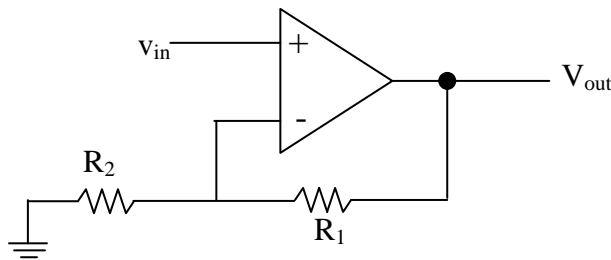
Prob. 3. Given the non-inverting amplifier shown below:

(a) Assume the open loop gain is A_o , then determine V_{out}/V_{in} as a function of A_o , R_1 and R_2 .

(b) Provide both the ideal V_{out}/V_{in} as well as the relative gain error “ ε ”. Ideal case $\varepsilon = 0$.

(c) Now assume the open loop is characterized by $\frac{GB}{s} = \frac{A_o \omega_{3dB}}{s}$, then

determine the expression $H(s) = \frac{V_{out}(s)}{V_{in}(s)}$.



This part of the problem deals with the numerical application.

(d) Assume the ideal voltage gain to be 21 and the relative gain error in % to be less than 2%, then determine the minimum DC open loop gain A_o .

(e) Determine the gain-bandwidth product GB for an ideal voltage gain of 21 and the settling time to be less than 10 ns. Hint: assume $A = GB/s$.