ELEN 607 (ESS) **Due: February 12, 2008**
Spring '08

HOMEWORK ASSIGNMENT #3

Prob. 1. Design a NGCC Amplifier with a differential input in 0.5μm CMOS technology for the following specifications. Use the one equation all region transistor model. Provide tables summarizing results and significant plots. Do not use CADENCE circuits figures in your report; draw your own (clean) circuit figures. Discuss the main results.

Power Supply	$\pm$1.0V or 2V
Load	10KΩ//6pF
Gain Bandwidth Product	$>$195MHz
DC Gain	$>$ 60dB
Phase Margin	$>50^{o}$
Setting Time	$<$90ns
Power Consumption:	$<$20mW
Slew Rate	$>$170 V/μs

Include a (general) design procedure, in particular provide enough details for the determination of the settling time and phase margin. Determine the slope factor "n" used in the one equation all regions MOS transistor model.* How did you determine the order of the amplifier? Write a MATLAB program to design your amplifier. Also, in your report, include results of CMR, CMRR(0), $PSRR^-$, $PSRR^+$, active area, process variations and SR.

Prob. 2. Design a multistage amplifier-frequency compensated (you can pick DFCFC1 [1] or DFCFC2) or a reversed Nested Miller compensation [2] that meets the specs of Problem 1, but uses at least 40% less power. Compare you results with the ones in Problem 1.

Prob. 3. (Extra Credit) Propose a new compensated multistage amplifier that could be one using a combination of techniques reported in the literature.

Prob. 4. Repeat the design of Prob. 1 but now using 65nm technology. The only differences in specs is that DC Gain > 55 dB and GBW > 950 MHz and power supply is 1.0 V. Furthermore, under unity gain close loop conditions apply a DC signal and sinusoidal signal of 0.3 V peak. The DC input should be sweep for three cases to make $v_{out,\,DC}$ = {0, -0.3V, +0.3V}. Under those three conditions determine the open loop characteristics of the DC gain and GBW. Summarize in a table all the results.

References:

[1] K.N. Leung and P.K.T. Mok, "Analysis of Multistage Amplifier-Frequency Compensation", *IEEE Trans. on Circuits and Systems I*, Vol. 48, pp. 1041-1056.

[2] G. Palumbo and S. Pennisi, "Design Guidelines for Optimized Nested Miller Compensation", *Southwest Symposium on Mixed Signal Design*, 2000 SSMSC, pp. 97-102.

* Plot I_D vs V_{GS} curve in weak inversion, and measure $\frac{1}{n} = \frac{d}{dV_{GS}}\{\ell n(I_D)\}$. Also determine from simulation of one transistor biased in the intended region the parasitic capacitance, g_m, g_o, and lambda.