

## HOMEWORK # 4

Prob.1. Design a voltage reference in 0.5 $\mu$ m CMOS technology based on weighted gate-source voltage difference between an NMOS and a PMOS [1]. Provide tables summarizing results and significant plots. The specifications are as follows:

Voltage Supply	1.5V
Power Consumption	15 $\mu$ W
Temperature coefficient (0 to 100 °C)	<30ppm/°C
PSRR@100Hz	>50dB
@10MHz	>25dB

[1] Ka Nang Leung, and Philip K. T. Mok, "A CMOS Voltage Reference Based on Weighted  $\Delta V_{GS}$  for CMOS Low-Dropout Linear Regulators", *IEEE Journal of Solid-State Circuits*, Vol.38, No.1, Jan.2003

Prob. 2. Line driver design problem:

A data application requires a line driver with the following specification.

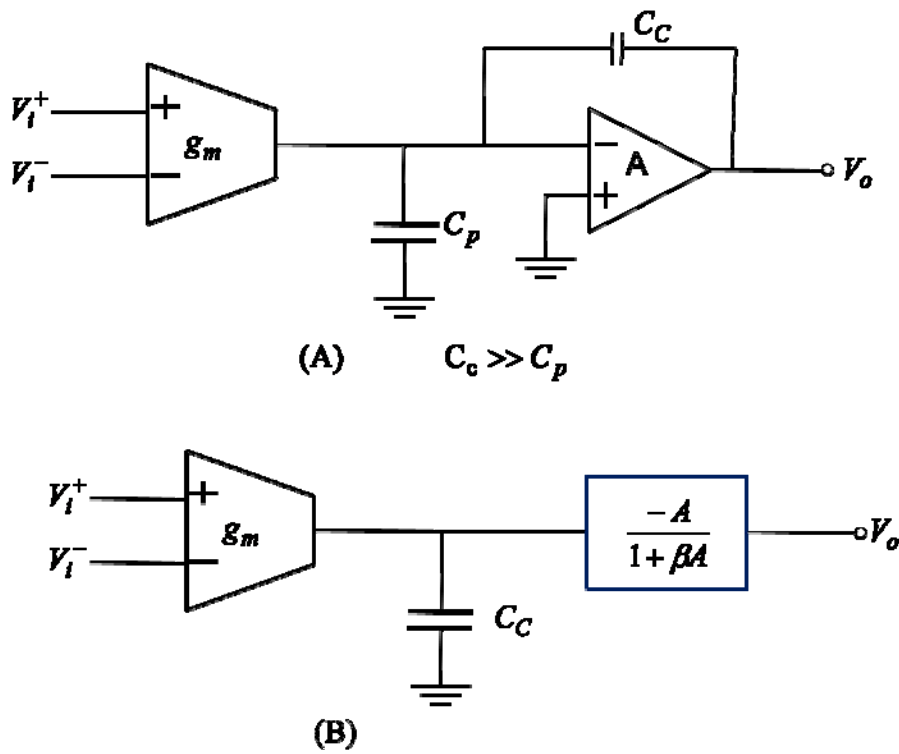
Parameter	Value
Load	8ohms    2pF
Supply voltage	+/-1.65V
Voltage swing	2.2Vpp
SNR (100KHz-1.2MHz)	>85dB
HD3 (2.2Vpp 1MHz tone)	<-76dB
Standby power dissipation	<100mW

The driver is intended to be used in an inverting configuration with Gain = -1.

- Compute the resistor values assuming 50% noise contribution from the input and feedback resistors and 50% noise contribution from the amplifier.

- b) Design the line driver using the 3-stage Class-AB amplifier architecture shown in the lecture notes (refer to 16Ω Headset driver example). Use TSMC0.35um technology and follow the design procedure outlined in the notes.
- c) All parameters must be simulated at 60C temperature. Ensure that Phase Margin is above 45° under quiescent condition.

Prob. 3.



Show that circuit (A) can be modeled as shown in circuit (B). Discuss the approximations needed for this approximation and the value of  $\beta$ . Write the exact transfer function of (A) and (B).