

ELEN 607 (ESS)  
Spring 2003

***Proposed Final Projects (Updated)***

These projects can be done by a team of one, two or three students.

All the circuits must include: a) Design methodology, b) Criteria for component value computation, c) Table summarizing results d) Layout and post layout simulations, e) Monte Carlo and temperature analyses.

**Project 1** (Chao, Jun, and Lin—May 2) Design a switched- Op Amp and show its functionality with a first-order SC LP filter. See ref. SSCC 2003, paper 23.2 “ A 0.9 V 0.5 uW CMOS Single-Switched-Op-amp Signal Conditioning System for Pacemaker Applications”. The design specifications are:

$A_{vo}$ (DC Gain)	>75dB
CMRR (at 100Hz)	>65dB
GBW	$\geq 50$ kHz
SR	max
Linear Output swing (SE)	0.5V
$C_L//R_L$	1pF//25K $\Omega$
$V_{SUP}$	$\pm 0.5$ V
Power Consumption	< 200 nW
Phase Margin(degrees)	> 56
TSMC 0.35 $\mu$ m CMOS	

**Project 2.** (Chinmaya, Pushkar, and Xiaohua—May 2) Design a low power multi-stage amplifiers with three or four stages operational amplifier. The architecture must be different from the ones reported in the literature. For reference see IEEE JSSC, No.3, pp 511-520, March 2003.

The specs to be satisfied are:

$A_{vo}$ (DC Gain)	>110dB
CMRR (at 100Hz)	>65dB
GBW	$\geq 4.5$ MHz
SR	$\geq 1.5$ V/ $\mu$ s
Area ( in mm <sup>2</sup> )	< 0.10
$C_L//R_L$	120pF//25K $\Omega$
$V_{SUP}$	$\pm 1$ V
Power Consumption	< 0.5 mW
Phase Margin(degrees)	> 60
AMI 0.5 $\mu$ m CMOS	

**Project 3.** (Wenchang, Jianlong and Xuemei—May 2) Design a very linear OTA S/N+D > 80dB, 65dB at 1 MHz and 20 MHz, respectively.  $V_{dd}=-V_{ss}=1.65$ V, 0.5 $\mu$ m AMI, Power Dissipation <10mW,  $C_L //R_L = 10$ pF // 25K.  $\phi_e < 2^\circ$  at 1.1 MHz.

Then design a first-order filter with a DC gain of 2, and 3dB cutoff frequency of 1.1 MHz, use phase compensation techniques.

**Project 4.** (Burak, Julio and Abraham—May 3) (Miguel, Angel Rojas—May 3) (Tianwei Li, A. Larsson, G. Zhang—May 3) At most one (1) external inductor is allowed in this project where an Class-D Amplifier design with the following specifications is required.

Ideal Channel Noise	-79dBm0
Leakage Current	< 1 uA
PSRR at 50 kHz	> 50 dB
THD	66dB @ 0dBm0, 69dB @ -3dBm0, 72dB @ -6dBm0, 75 dB @ -10dbm0
Maximum signal swing (Differential 0 dBm0)	4.6V <sub>pp</sub>
C <sub>L</sub> /R <sub>L</sub>	100 pF//8 Ω
V <sub>SUPPLY</sub>	2.7V
Power Consumption Efficiency	< 500 uA > 90 %
TSMC 0.35μm CMOS	

**Project 5.** (Yang, Jin-Yi and Nikolaos—May 3) Design a Digital to Analog Converter (DAC) using floating gate techniques, in 0.18 um CMOS technology. The calibration scheme can be implemented at the system level and tested with the transistor FG circuit implementation. Discuss the actual implementation of the calibration scheme. The approximated specifications are:

Max Sample Frequency	200	MS/s
Resolution	8	bits
DNL	+/- 0.25	LSB
INL	< 1	LSB
SFDR	<-75 (limited)	dBc
IMD (to 150 MHz)	<-80	dBc
NSD	<-160	DBm/Hz
Power	< 300	mW
Area	< 2.2	mm <sup>2</sup>

**Project 6.** (Sangwook and Choonghoon—May 1) Following the approaches to design fully balanced, fully symmetric OTA done by Praveen and Ahmed, design a fully differential Op Amp based on single-ended Op Amps without doubling the area and power consumption. Use a class AB for the output stage(s). The specifications are:

$A_{vo}$ (DC Gain)	>86dB
CMRR (at 100Hz)	>70dB
GBW	$\geq 6$ MHz
SR *	$\geq 4$ V / $\mu$ s
Area ( in mm <sup>2</sup> )	min
$C_L//R_L$	20pF//0.5K $\Omega$
$V_{SUPPLY}$	$\pm 1.65$ V
Power Consumption *	< 6 mW
Phase Margin(degrees) *	> 66
AMI 0.5 $\mu$ m CMOS	

\* These specifications might be modified if needed.

**Project 7.** (David Báez-Villegas—May 1) To design, simulate and layout a two-stage rail-to-rail input ( and output) operational amplifier using AMI 0.5 CMOS technology to meet the following specifications with class AB output stage:

$A_{vo}$ (DC gain)	>90 dB
GBW	> 6 MHz
PM (Phase Margin)	> 60°
SR (Slew Rate)	> 4 V/us
$V_{outpp}$	> 3 V
$C_L$	20 pF
$R_L$	10 k
$P_D$	< 8 mW
$V_{supply}$	+/- 1.65V

**Project 8.** (Arun—May 1) Design a Buffer Amplifier, that meets the following characteristics:

The process technology is up to you to be selected.

- 1)  $I_d$  (per amplifier not including the Bias) < 12 $\mu$ A
- 2) Area  $\leq 26\mu\text{m} \times 400\mu\text{m}$
- 3) Settling Time  $\leq 8\mu\text{s}$  to 8 Bit
- 4) Analog Supply  $11\text{V} < V_{dda} < 17\text{V}$
- 5) CMR=  $\text{gnd}+0.2$  to  $V_{dd}-0.2$
- 6) Load  $50\text{pF} < C < 150\text{pF}$   
 $1\text{k} < R < 30\text{k}$
- 7) DC open loop gain 70 dB
- 8) Phase Margin 75 deg

**Project 9** (Janelle Tonti—May 1) >1 . Built-in Buffer for testing purposes capable to satisfy the following specifications:

- >Max input capacitance: < 100 fF
- >Output impedance: =< 50 OHM
- >3db Cut-off frequency: >= 2.4 GHZ
- >Maximum Output signal: 400 mVpeak-peak
- >Power Supply: 0-3 V
- >CMOS Technology 0.35 um
- >Power Consumption( maximum)< 6 mW

**Project 10.** (Feyza, Sualp and Rida—May 2)

Design a Fully Differential S/H Circuit.

Note below that 14 dB Gain is an important figure for pipeline ADCs because is the typical gain of the multipliers by 2 when you include all parasitic effects. The specifications are:

*AC Performance*

- DC gain 108 dB
- Bandwidth at 14 dB 217 MHz
- Phase margin at 14 dB 63
- GBW at 0 dB 800 MHz
- PHASE MARGIN AT 0 dB > 48 DEGREES

*Transient (gain=4)*

- Settling time <3.5 ns (0.1 %)
- Slew rate >110 V/ s

*Output Swing*

- +/- 500 mV
- >CMOS Technology 0.35 um
- SUPPLY VOLTAGE +/- 1.5 V

The important dates are:

**Progress Report (April 14, 2003)** with discussion of the specifications, clearly define the problem, preliminary simulations and identification of the future work and a summary of the reported related publications in the literature. No more than 10 pages. This report is worth 10% of the final project. This (word document) report **must** have the following form:

Title

Statement of the problem

Background, previous work

Potential applications of your circuit provide specific examples and references.

Basic idea of your solution. Preliminary Results

Problems to be solved in the near future.

**References, a complete list of references must be included.**

**Final Written Report (May 7, 2003). This final (word document) report, following IEEE Journal of Solid-State Circuit format style must include:**

1. Title
2. An abstract
3. Introduction
4. Background and a comparative table of previous results
5. Proposed Solution
  - • Circuit Diagram and explanation
  - • Design Procedure, how to determine the (W/L)'s
  - • The temperature, noise and process variation effects
6. A Comparative Table between Hand calculation and Simulation
7. Discussion of Results and suggested improvements.
8. Layout of the Circuit
9. References

**Oral Presentations in PowerPoint Form: May 1\*, 2\* and 3<sup>+</sup>, 2003**

\* Room 326, Reed-McDonald

10:00 – 12:30 p.m.

+ Room 127A ZEC

10:00 – 12:30 p.m.