

Lab 1

Three-Stage Operational Amplifier

Objective:

To design, simulate, layout and test a three-stage Operational Amplifier. The lab work will also include postlayout simulation with the parasitic components extracted from the layout.

Circuit Description:

The schematic of the circuit is given below as Fig. 1. It is a three-stage Operational Amplifier. The first stage is a differential pair with NMOS input transistors and PMOS current mirror load. The second stage is a PMOS common source gain stage and the last stage is a class AB push-pull output stage. Note that the diode connected transistors M_9 and M_{10} are used to bias the output source follower transistors at class-AB. A Miller compensation capacitor C_c is added to the second stage to ensure stable operation of the amplifier in closed loop.

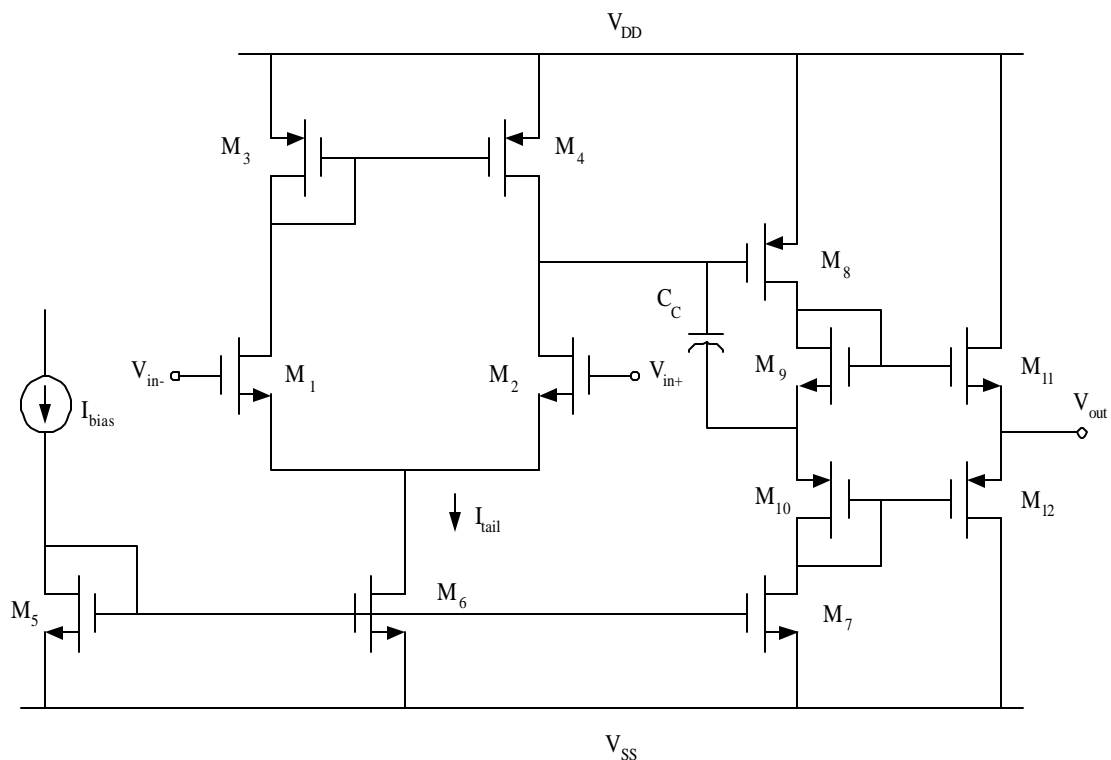


Fig.1 Three-stage operational amplifier

Prelab:

Design the operational amplifier of Fig.1 with AMI 0.5 μ m CMOS technology to comply with the following specifications:

A_{vo} (DC gain)	> 60 dB
CMRR (at 100 Hz)	> 70 dB
GBW	> 10 MHz
PM (Phase Margin)	> 45°
SR (Slew Rate)	> 2V/ μ s
CMR	> 1V
V_{outpp}	> 0.8 V
R_{out}	< 1k Ω
C_L	30pF
R_L	1k Ω
P_D	< 0.8mW

Note:

- 1) The power dissipation specification does not include the bias current source.
 $V_{dd} = |V_{ss}| = 1.5V$.
For a sample design procedure, you can refer to the documentation on Lab 8 of ELEN 474 Laboratory from the following web site:
<http://amesp02.tamu.edu/~afmondra/elen474/lab31111.htm>
At the end of the web site given above, you will see a link to a pdf file called “Maple Program for the design of the Three Stage Operational Amplifier”.
- 2) As the time of our lab class is pretty tight to finish all the design, simulation, layout and extraction work. Very careful preparation for the prelab is essential for the success of the lab. Please capture the schematic with Cadence Composer and try to simulate DC, AC, and transient performance of the amplifier using Spectre within the Analog Artist Environment of Cadence, and check whether the specifications are met. You may have to do some fine tuning using the simulator to meet the specs. If you cannot meet a spec, justify this.
- 3) In the prelab report, please include
 - a) The detailed design procedure for the amplifier. Please tabulate the key design parameters, like (W/L)’s and bias currents of the transistors. Please name the transistors exactly the same as Fig. 1.
 - b) Preliminary DC, AC and transient (SR) simulation results, including, i) DC input referred offset; ii) input output characteristic plot of the amplifier (DC sweep); iii) Frequency response of the amplifier (AC sweep), please indicate GBW and phase margin in the AC plot; iv) SR simulation plot

Lab:

• Week 1 (Jan. 21) Simulation and Layout

SpectreS simulator within the Analog Artist Environment of Cadence will be used throughout all the simulations in the lab. All the simulation results should be included in the final report.

- 1) Simulate the DC, AC, CMRR and SR performance of the amplifier.
- 2) Simulate the noise performance of the amplifier. Obtain the noise summary (spot noise at $f=100\text{Hz}$ and the integrated noise from $f_1=1\text{Hz}$ to $f_2=1\text{MHz}$.), the plots of the equivalent output noise voltage spectral density and the equivalent input noise voltage spectral density. Sweep the temperature from -40C to 100C in the noise analysis at $f=100\text{Hz}$ and observe how the input and output noise change with temperature.
- 3) Simulate the noise-power consumption trade-off using the noise simulation and the parametric analysis tools together. For this simulation, use the bias current of the opamp as a parameter. Obtain the noise summary (spot noise at $f=100\text{Hz}$ and the integrated noise from $f_1=1\text{Hz}$ to $f_2=1\text{MHz}$.), the plots of the equivalent output noise voltage spectral density and the equivalent input noise voltage spectral density. What is your observation? Elaborate on the trade-off that you observe in your final report.
- 4) Simulate the THD of the opamp for an input voltage of 2mV_{pp} at $f=1\text{kHz}$. What is the maximum input voltage that you can apply to your opamp for 1% THD at the output voltage? Using this value and the integrated equivalent input noise voltage that you obtained in the previous section, calculate the Signal-to-Noise Ratio (SNR) of the opamp.
- 5) Set the width of the driver transistors of the input differential pair as a design variable. Keep the bias current constant and simulate the THD and the noise performance of the opamp using the parametric analysis tool with the width of the transistors being a parameter. Can you observe a trade-off between noise and THD for a given power consumption? Elaborate on the trade-off that you observe or that you would expect in your final report.
- 6) Run a Monte Carlo Simulation of the opamp design. Vary the parameters V_T , K_P and LAMBDA by 20% with a Gaussian distribution and Random Variations. Generate a histogram for the following parameters:
 - GBW
 - P_D
 - PM
 - A_{v0}

Comment on the impact of the process variations on each of these parameters.

- 7) Create a layout cell view for your opamp. Layout your final design using common-centroid arrangements for the transistors that are to be matched. In your final report, make sure that you indicate the transistors to be matched. Use the

layout vs. schematic checker and include the “net-lists match” page in your final report. Extract your layout using the Extractor and run the same simulations as those in the first part of Lab Week 1 and comment on the differences between the prelayout and postlayout performances of the circuit.

- **Week 2 (Lab Measurement)**

The circuits were designed with CMOS 2 μ m Orbit Technology and were fabricated through MOSIS. The characteristics of the circuits to be measured are power consumption, output offset voltage, input offset voltage, slew rate, input common-mode range and output resistance. Circuits will be loaded with a capacitance of 30pF in parallel with a resistor of 1k Ω . Note that the value of the explicit capacitor that will be connected to the output should be determined so as to provide a total capacitance of 30pF at the output taking the probe and the input capacitances of the oscilloscopes. Although some sample test configurations will be provided on a separate sheet during the lab, you are allowed to use whichever test configuration you deem suitable for the characterizations. The results together with the schematics of the test configurations which are used to obtain the measurements should be documented in the final report properly.

The characteristics of the operational amplifier which will be measured in the lab were obtained as follows in the postlayout simulations in the design phase:

Output offset voltage:	686mV
Input-referred offset voltage:	0.68mV
Input CMR:	-0.9V to 0.7V
SR+:	2.54V/ μ s
SR-:	1.59V/ μ s
Output resistance at DC:	66?
Power Consumption:	2mW

The circuit has a dual power supply of $V_{dd}=|V_{ss}|=2.5V$.

An circuitry designed in the same 2 μ m technology will be provided in class. It is vital that you include a comparison table in your final report showing the measured characteristic and its value obtained in the postlayout simulations as given above.

Below is the pin diagram and testing setup for the chip.

