

A Nonlinear Macromodel for CMOS OTAs

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Abstract

A nonlinear parameterizable macromodel for CMOS Operational Transconductance Amplifiers (OTAs) is presented. The macromodel captures the DC, AC and large signal features of the transistor level original circuit, thus modeling accurately its time domain and nonlinear performance. The main contribution of this work is to account for the bias-dependent transconductance nonlinearities in the circuit, by curve-fitting the desired output characteristics with n -dimensional polynomials. The model can also account for the nonlinear dependence of the circuit's characteristics on several design parameters. The applicability of the model is demonstrated by modeling the response of an OTA-C filter.

I. Introduction

Circuit simulators like HSPICE are very useful tools for any IC designer, but the simulation of complex mixed-signal systems at the transistor-level is prohibited by the computational cost and potential convergence problems. To reduce the computational overhead and improve the simulator convergence, macromodels have been used for many years when simulating big subsystems and systems.

Macromodels are just simplified circuit descriptions whose behavior resembles very closely that of the transistor-level circuit, but use less and simpler components. A macromodel should be as simple as possible, model accurately the desired characteristics, reduce the simulation time and improve the convergence of the simulator. Almost any circuit [1]–[4] can be macromodeled using either one of two methods: a simplified circuit description or a behavioral macromodel.

Historically, op-amp macromodels began with the "Boyle" model [1] in 1974, which used an actual differential pair to model the nonlinear large-signal response of the amplifier, an intermediate stage and an output stage. In most cases a macromodel is split into an *input stage* (to model the input characteristics, including the input nonlinearities), one or more *intermediate stages* (to model the gain and the frequency response by modeling the circuit's poles and zeros) and an *output stage* (to model the output swing, output impedance, etc.). A good comparison study of the existing popular op-amp macromodels can be found in [4].

Initially, macromodels were aimed at BJT-based op-amps, but as technology has evolved, more analog functions are implemented using CMOS technology. Thus, several macromodels have been developed for CMOS op-amps [5] and for CMOS OTAs [6] in the recent years.

II. Generic OTA Macromodel

The OTA macromodel presented here (Fig.1) is based on an existing op-amp macromodel [2]. It has been modified to better model the very high input impedance of CMOS

circuits, to decouple the common and differential mode gains, and to allow for the introduction of *nonlinearities*, while keeping the model as simple as possible. The macromodel is composed of several stages as shown in Fig.1.

Input Stage

For the input stage, it has been assumed that the DC differential and common mode impedances are infinite. For common mode, the input impedance is just the input capacitance, which can easily be extracted from HSPICE simulations and is given by: $C_{INcm} = 2C_{cm}$

The differential mode input impedance has poles at:

$$\omega = 0, \text{ and } \omega = \frac{C_d + C_m}{R_d C_d C_m} \quad (1)$$

and a zero at: $\omega = \frac{1}{R_d C_d}$

This stage also includes an input DC offset source (V_{os}).

Common mode stages

To model the AC response of an OTA, both the common mode and the differential mode responses must be taken into account. In the model of Fig. 1, the common mode signal is detected by averaging the input voltage over the input capacitors (C_{cm}). Two zero stages are provided exclusively for the common mode response and an additional zero and two more poles are common to both differential and common mode responses.

For the common mode zeros included in Fig. 1, both RL sections are characterized by similar transfer functions in the frequency domain. The zero stages produce a zero at R_1/L_1 and a zero at R_2/L_2 .

Gain and second Pole stage

In the gain stage, the common mode (CM) and the differential mode (DM) gains are modeled through the current sources I_{dm} and I_{cm} . Besides the transconductance gain, this stage models also the second pole of the OTA, given by $(R_3 C_3)^{-1}$.

For the nonlinear model, I_{dm} and I_{cm} become nonlinear sources which depend on several independent variables. In the simplest case, only the dependence of I_{dm} on V_{idm} and the dependence of I_{cm} on V_{icm} are considered. Additionally, the current sources I_{dm} and I_{cm} can be made dependent on several other design variables and/or parameters (e.g. W/L of input transistors, additional biasing sources, etc.), by using n -dimensional functions.

Intermediate stages

To reproduce the actual frequency response to the desired accuracy, several pole and zero stages are added after the gain stage (*Intermediate stages*). Each of these additional stages provides unity gain. If needed, an *all pass* stage can be added to better model the phase response characteristics.

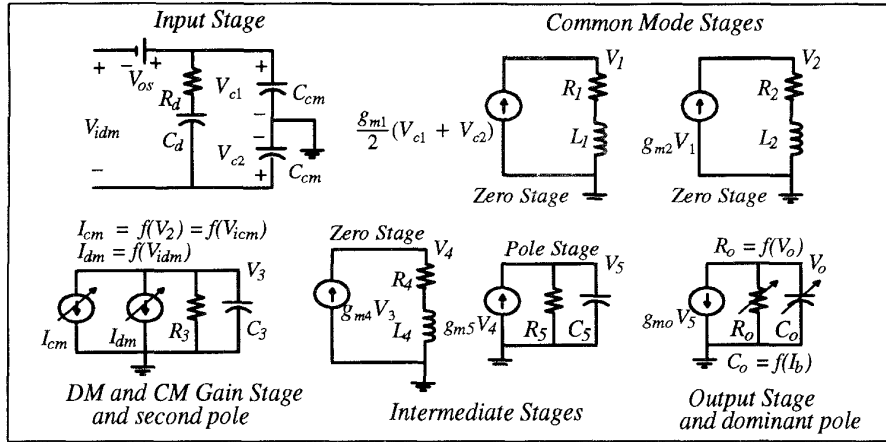


FIG. 1 GENERIC OTA MACROMODEL

Output Stage

In the last stage, the output impedance, the output swing and the dominant pole are modeled using a simple RC circuit. But both the output resistor and the output capacitor can be nonlinear elements, to account for the output voltage swing and the frequency dependence of the dominant pole.

The main contribution of this paper is to offer a simple way to model the nonlinear dependence of the output current on both the input voltage and the biasing current. This allows for using the proposed macromodel for circuit tuning and optimization purposes, while taking into account the large signal input nonlinearities. Additional parameters like the W/L of the input transistors, the biasing of the output cascode (if any), the gain of the current mirrors, etc., could also be included as independent parameters, depending on the intended application. It should be noticed that the proposed model is extracted from simulated output results, what makes it independent from the transistor-level architecture.

III. Extraction of the macromodel parameters

To illustrate the accuracy of the presented model, the simple two-stage OTA shown in Fig. 2 is used as an example.

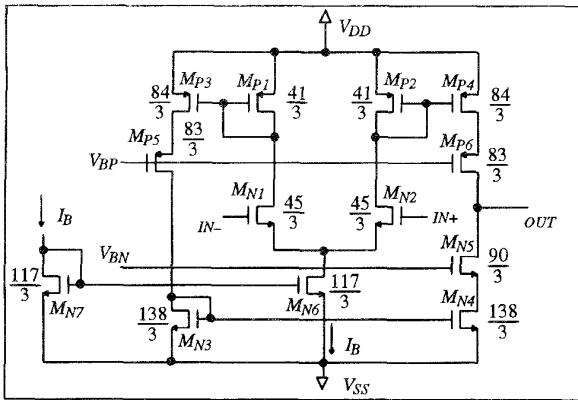


FIG. 2 OTA CIRCUIT

A. Linear Model

This circuit was simulated in HSPICE with $I_b = 120\mu A$, $V_{BP} = 1V$, $V_{BN} = -1.5452V$ and $V_{dd} = |V_{ss}| = 4V$. The circuit

parameter values obtained from the simulation of the OTA, using $V_o \sim 0$, are listed in Table I.

TABLE I. HSPICE SIMULATION DATA

Parameter	Simulated Value
g_{mdm} DM Transconductance	596.04 $\mu A/V$
g_{mcm} CM Transconductance	56.41 $\mu A/V$
A_{vdm} DM V/V Gain @ DC	1239.40 \rightarrow 62.2dB
CMRR CM Rejection Ratio	10565.95 \rightarrow 80.4dB
R_o Output Resistance	2.17 M Ω
Φ_e Phase Error @ 1MHz	1.75 $^\circ$
ω_{p1} Dom. pole ($2\pi f_{p1}$)	$2\pi(666.95$ KHz)
ω_{p2} 2nd pole ($2\pi f_{p2}$)	$2\pi(56.16$ MHz)
ω_{p3} 3rd pole ($2\pi f_{p3}$)	$2\pi(77.69$ MHz)
ω_{z1} Zero ($2\pi f_{z1}$)	$2\pi(77.94$ MHz)
ω_{zcm1} 1st CMZero ($2\pi f_{zcm1}$)	$2\pi(813.67$ KHz)
ω_{zcm2} 2nd CMZero ($2\pi f_{zcm2}$)	$2\pi(2.77$ MHz)
Z_{idm} DM $Z_{in} \rightarrow$ Real part	1112.10 Ω
Z_{idm} DM $Z_{in} \rightarrow$ Imag.	-1.58 E09
$ Z_{icm} $ CM Z_{in} @ LF	2.85 E09
$\angle Z_{icm}$ CM Z_{in} : Phase	90 $^\circ$

To compute the values of the input-stage elements, some additional formulae are needed:

$$C_{cm} = \frac{1}{4\pi f_1 |Z_{icm}(f_1)|} \quad C_d = \frac{1}{2\pi f_1 Z_{idm} |Im|_{f_1}} - C_{cm} \quad (2)$$

$$R_d = \frac{Z_{idm} [Re](C_d + C_{cm})^2}{C_d^2}$$

To find the other element values in the macromodel, the pole and zero equations mentioned in Section II are used, together with the pole-zero analysis in HSPICE. As the overall gain is lumped in the gain stage, all the other stages should provide unity gain. The calculated element values for this example are shown in Table II.

The results of the macromodel simulation in HSPICE follow closely those of the transistor-level circuit simulation up to 20 MHz, as shown in the transconductance gain vs frequency response plot depicted in Fig.3. If a better correspondence is wanted at higher frequencies, more pole-zero stages must be added, mainly to correct for the phase errors

TABLE II. CALCULATED PARAMETER VALUES

Element	Value
C_{cm}	27.88 fF
C_1	72.70 fF
R_d	2128.50 Ω
$R_1=R_2=R_3=R_4=R_5$	1K Ω
$g_{m1}=g_{m2}=g_{m3}=g_{m4}=g_{m0}$	1mmhos
L_1	125.60 μ H
L_2	57.38 μ H
C_3	2.83 pF
L_4	Not used
C_5	2.05 pF
R_0	2.17 M Ω
C_0	109.88 fF
I_{dm}	$g_{mdm}=590.04 \mu$ A/V
I_{cm}	$g_{mcm}=56.41 \eta$ A/V
V_{as}	-1.44 mV

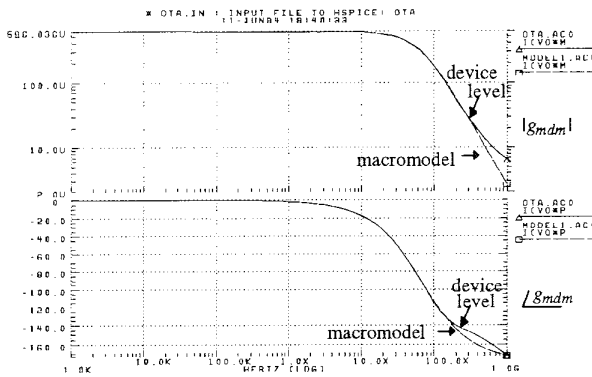


FIG 3 DIFFERENTIAL TRANSCONDUCTANCE GAIN

B. Nonlinear Model

The proposed macromodel can be greatly enhanced by including several nonlinearities inherent in the transistor-level circuit. The procedure followed to include those nonlinearities can be summarized as follows:

Collection of the necessary transistor-level simulation data

To obtain the input data a parameter space must be generated from the transistor-level simulation, so that the desired function values (e.g. I_{dm} , etc.) are known for all permutations of the input variables. An HSPICE post-processor module written in C was developed to compile the input data space.

Fitting of an n-dimensional surface to the simulation data

This is done by finding the polynomial that better conforms to the data, minimizing the error in some statistical sense (for example in the Least Squares sense). For the example of $I_{dm}=f(V_{idm}, I_b)$, the polynomial to be found is of the form:

$$I_{dm} = \sum_{i=1}^N a_i V_{idm}^\alpha I_b^\beta \quad (3)$$

where the values of α and β must be carefully determined. For the surface fitting, an HSPICE Pre- and Post-processor (HPP) software package [7] was used.

Surface Splitting and fitting

The functions that model the large signal behavior of electronic circuits are highly nonlinear, creating abrupt changes of curvature in the characteristic functions. A curve

with abrupt changes is difficult to model by direct polynomial fitting [8]. For the purpose of this work, a compromise between high-order polynomial and spline fitting has been adopted. A given curve/surface is split into several segments/regions where the curvature remains relatively unchanged. Each of these segments/regions is fitted with low-order polynomials to ensure stability.

Initially, the first and second derivatives of a surface in a given direction are obtained numerically. Then, these derivatives are smoothed by median filtering to eliminate most discontinuities in the data. Next, the curves/surfaces are split into regions where the curvature remains relatively unchanged. Once the curves/surfaces have been split into regions at the points of maximum curvature, each segment is extrapolated to smooth its borders and finally, the curve fitting program can be applied to each of these regions, fitting using only low-order n-dimensional polynomials.

As a last step, the obtained polynomials must be included into the macromodel of Fig. 1. In HSPICE this was done by using polynomial sources with variable MIN and MAX limits.

IV. Example: differential nonlinearities of an OTA

To model the dependence of the differential mode output current on the input voltage (V_{idm}) and the bias current (I_b), a set of simulations were performed. From these simulations, a parameter space as a set of I_{dm} vs V_{idm} curves with I_b as parameter is obtained, as shown in Fig. 4. Each curve is split into four regions (I to IV in the figure) to allow for fitting with low-order polynomials.

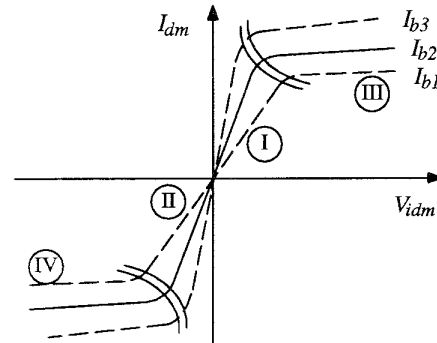


FIG. 4 DC TRANSCONDUCTANCE VS V_{IDM} AND I_B

The resulting fitting surface for a specified accuracy of 95% is shown in Fig. 5. As can be seen the fitting is very good in both V_{idm} and I_b directions inside the specified ranges.

The modeling in HSPICE was done by using two polynomial sources, and using the MIN and MAX options of the polynomial source card to model regions III and IV.

This procedure can be applied to model any nonlinear function in any kind of circuit, once the fitting and splitting tools are available.

V. Applications

The applications of this type of macromodel are quite numerous, since it allows modeling the transistor-level circuit for DC, AC and transient analysis. As the model also allows introducing several dependencies on design variables or input parameters, it is quite useful for design, optimization and tuning of analog circuits and systems. To show the

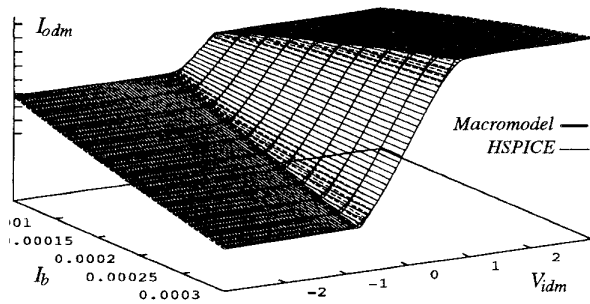


FIG 5 DC TRANSCONDUCTANCE GAIN WITH I_B AS PARAMETER

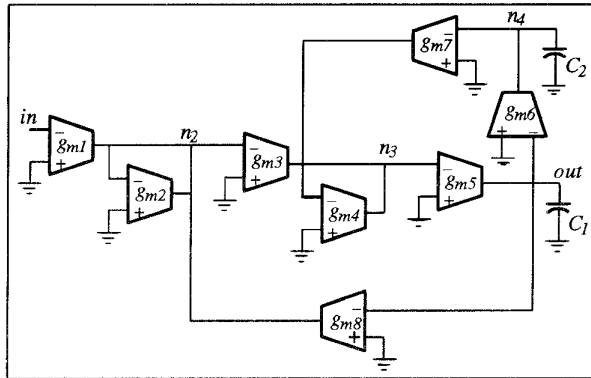


FIG. 6 OTA-C BIQUAD CONFIGURATION

model's capabilities and accuracy, it has been used to simulate a simple OTA-C continuous-time biquad Band-Pass filter, shown in Fig. 6. A simple filter was designed to render a center frequency between 200KHz and 800KHz, by varying g_{m5} and g_{m6} between $230\mu\text{A/V}$ and $920\mu\text{A/V}$. This is done by varying I_b between $20\mu\text{A}$ and $300\mu\text{A}$ in the OTA shown in Fig. 2.

The transient response to a sinusoidal input is shown in Fig. 7. As can be seen, the macromodel follows closely the transient response of the transistor-level circuit simulation at different frequencies. When a large signal is applied and the output current saturates, the macromodel is still in good agreement with HSPICE and the nonlinear output due to the slew rate of the OTA is also well simulated thanks to the current saturation capability of the model, as shown in Fig. 8.

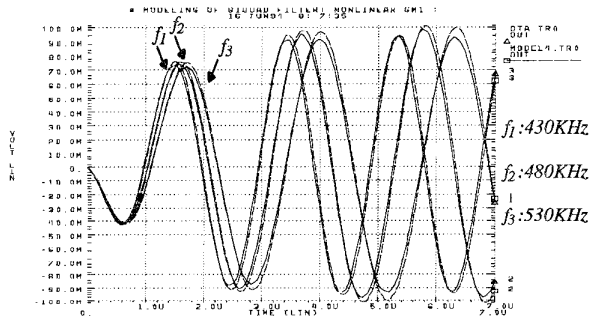


FIG. 7 TRANSIENT SIMULATION: OUTPUT VOLTAGE

As shown with these simulations, the proposed macromodel works quite well for simulating the time domain behavior of

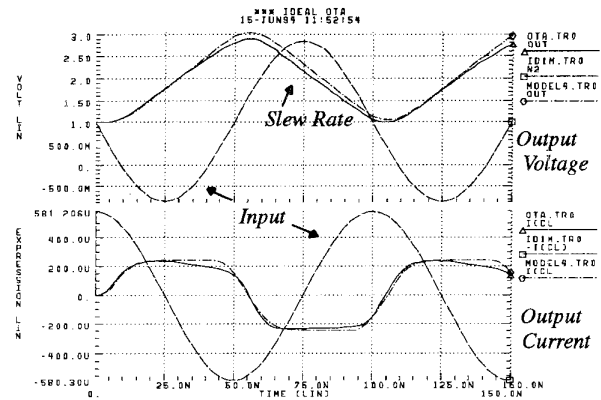


FIG. 8 LARGE SIGNAL SIMULATION

the transistor-level circuit, using less and simpler components.

Conclusions

A macromodel that can accurately simulate the time domain and large signal characteristics of any CMOS OTA circuit has been developed. The macromodel also allows simulation of the linear small signal characteristics and accounts for the differential and common mode input impedances of the amplifier. By comparing the macromodel performance against the transistor-level circuit's HSPICE simulation results in several examples, the macromodel has been shown to mimic quite closely the performance of the original transistor-level circuit, while accounting for nonlinearities and dependencies on several input parameters.

A systematic procedure has been devised to fit the nonlinear dependencies of any output function on the input parameters, to n-dimensional polynomials that can be modeled in HSPICE by using nonlinear polynomial sources. The feasibility of the fitting and its accuracy has been demonstrated with a system level simulation example.

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