Highly Linear Low Noise Amplifier

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Outline

- Motivation
- Background
- Proposed Solution
- Testing Strategy
- Experimental Results
- Conclusion

Motivation

- Numerous co-existing wireless standards and wireless equipment

Palm Powered devices support LAN, WAN, and PAN

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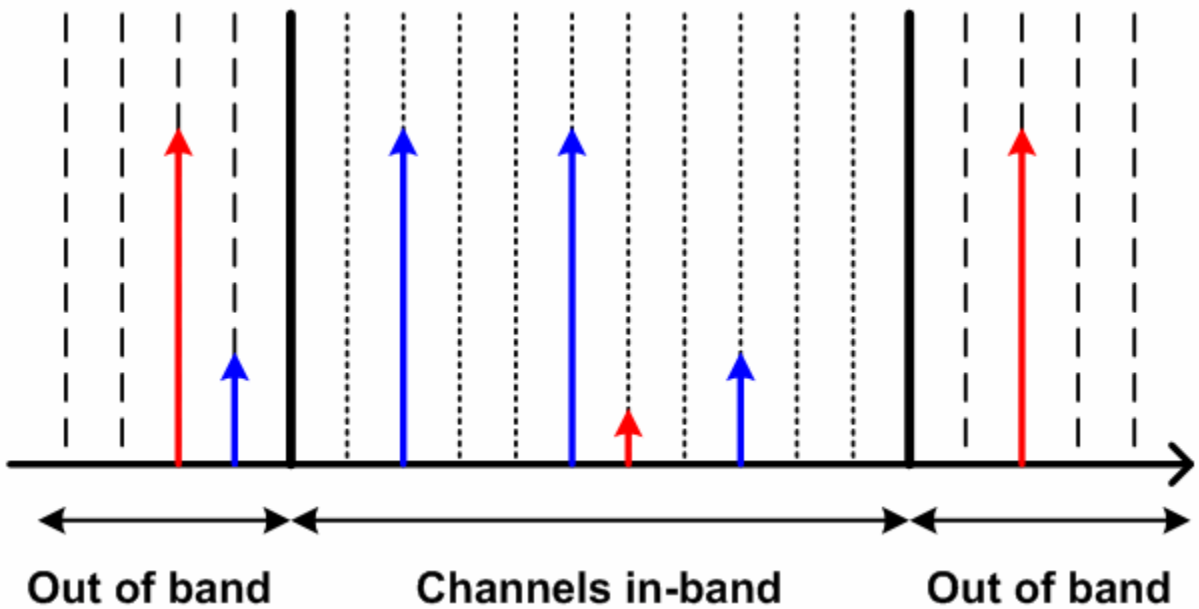
Frequency Spectrum

- Limited spectrum allotted to each user
- Possible large interferers from other channels in-band and out of band



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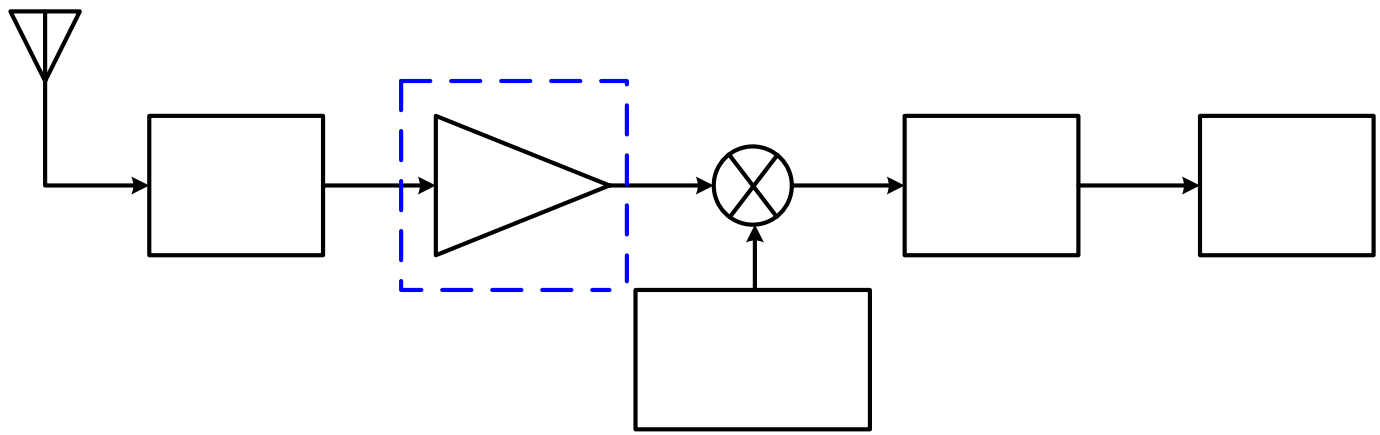
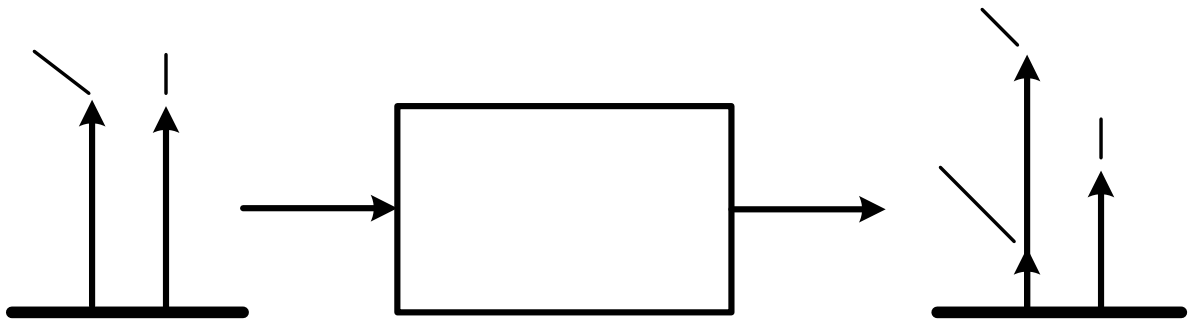
Receiver Architecture



- Antenna receives the entire band of signals
- Stringent requirements on the receiver front-end
- BPF filters the out of band channels
- LNA receives the entire in-band signals
- In-band channel interference problems in LNA
  - Blocking
  - Intermodulation

Blocking



$$y(t) = \alpha_1 x(t) + \alpha_2 x^2(t) + \alpha_3 x^3(t)$$

$$x(t) = A_1 \cos \omega_1 t + A_2 \cos \omega_2 t$$

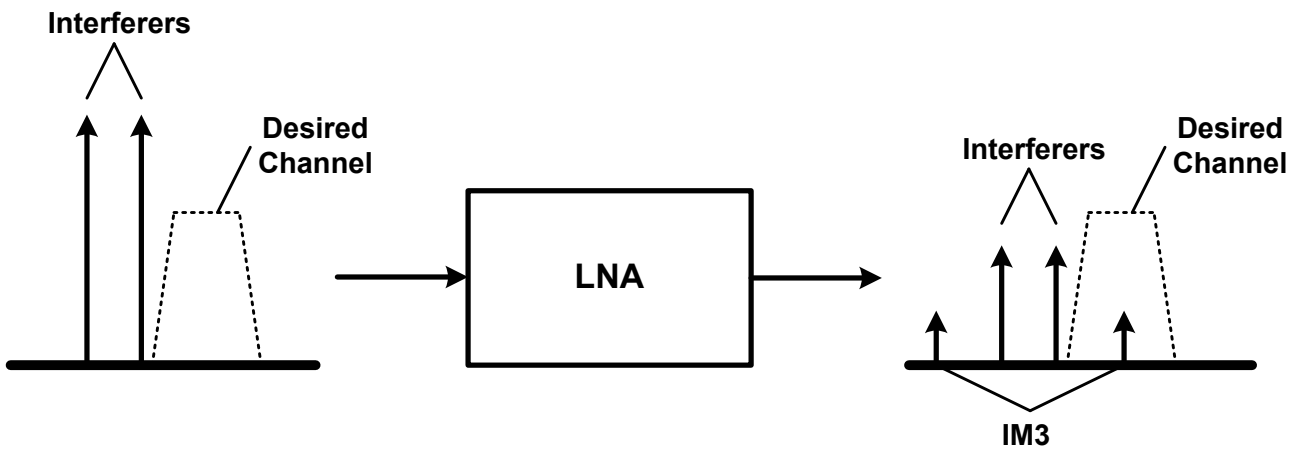
$$y(t) \cong \left(\alpha_1 + \frac{3}{2} \alpha_3 A_2^2 \right) A_1 \cos \omega_1 t + \ldots\ldots$$

– If $\alpha_3 < 0$, a large interferer results in signal being "blocked"

Desired

Interfe

Intermodulation



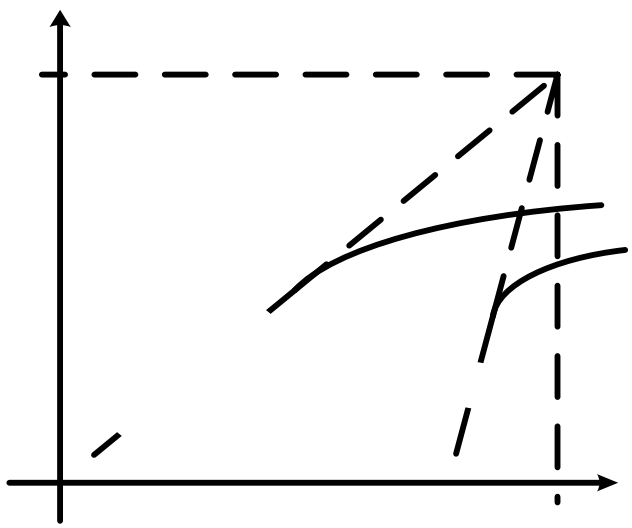
$$x(t) = A_1 \cos \omega_1 t + A_2 \cos \omega_2 t$$

$$y_{IM3}(t) = \frac{3}{4}\alpha_3 A_1^2 A_2 \cos(2\omega_1 - \omega_2) + \frac{3}{4}\alpha_3 A_2^2 A_1 \cos(2\omega_2 - \omega_1)$$

- Third order intermodulation (IM3) components corrupt the signal resulting in distortion

Linearity Measurement

- Third order Input Intercept Point (IIP3) is a measure of circuit non-linearity
- Fundamental = $\alpha_1 A$,IM3 = $\frac{3}{4}\alpha_3 A^3$



Low Noise Amplifier

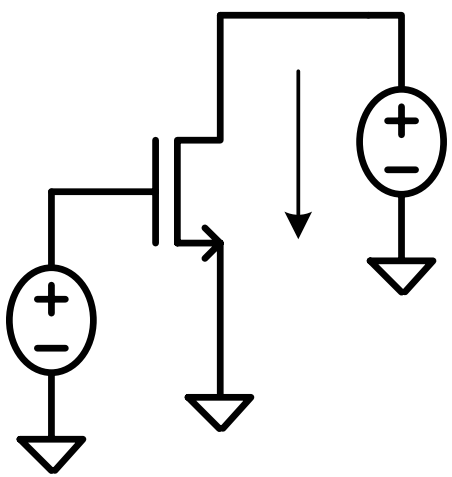
- Low Noise Amplifier
  - First amplifying block in a receiver
  - High gain, Low Noise Figure
  - Presents amplified signals (desired + IM3) to mixer
- Highly linear LNA with high gain and low NF required

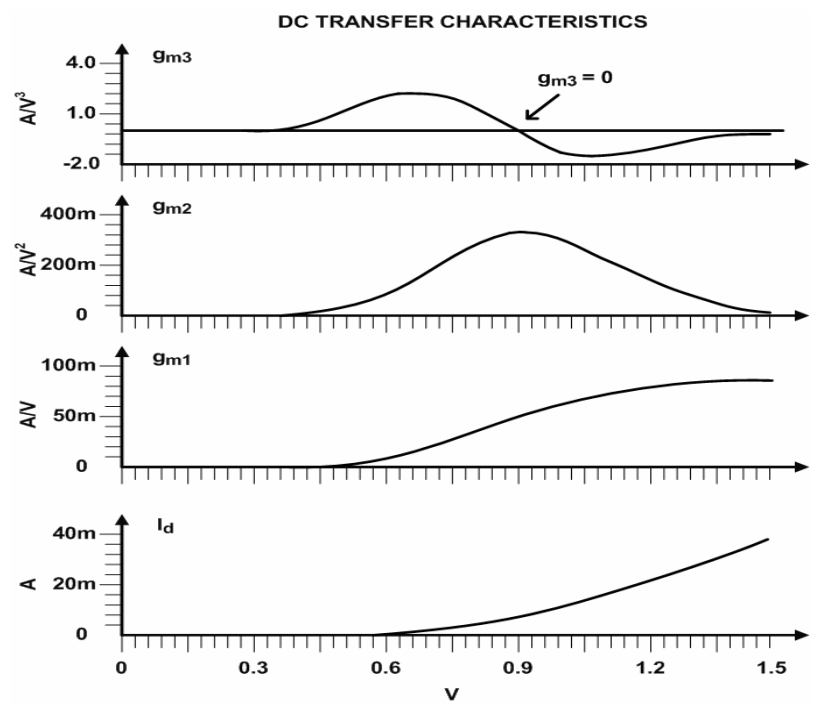
Background

- Existing Linearization Techniques
  - Optimum Biasing
  - Negative Feedback
  - Input Impedance Frequency Termination
  - Feedforward Cancellation

Optimum Biasing

- Current = $i_d = g_{m1}v_{gs} + g_{m2}v_{gs}^2 + g_{m3}v_{gs}^3 + ...$
- IIP3= $\sqrt{\frac{4}{3}\left|\frac{g_{m1}}{g_{m3}}\right|}$
- g_{m3}=0 results in very high IIP3



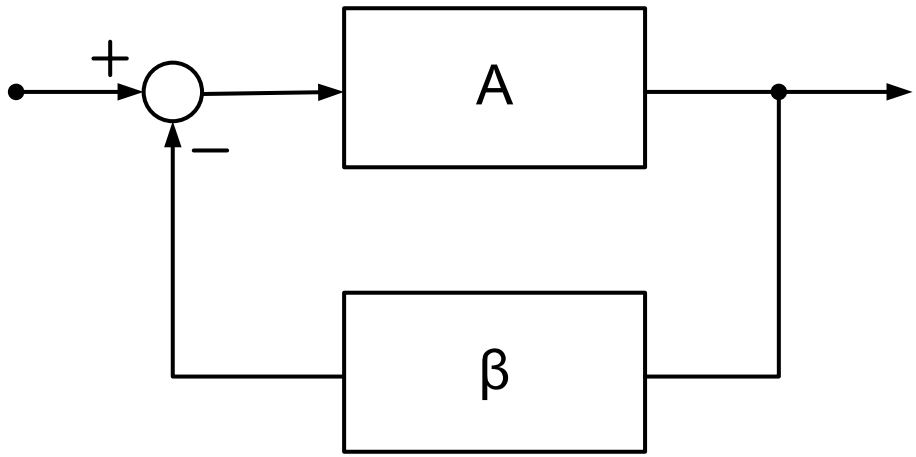


Optimum Biasing

- Drawbacks
  - High IIP3 obtained over a narrow region
  - Process variations degrade IIP3
  - Limited voltage gain due to restricted input transconductance (g_{m1})
  - Poor NF

Negative Feedback

- Popular in baseband circuits to improve linearity



- IIP3= $\sqrt{\frac{4}{3}\left|\frac{g_{m1}}{g_{m3}}\right|\frac{(1+T_o)^3}{\left(1-\frac{2g_{m2}^2}{g_{m1}g_{m3}}\frac{T_o}{1+T_o}\right)}}$, $T_o = g_{m1}\beta$

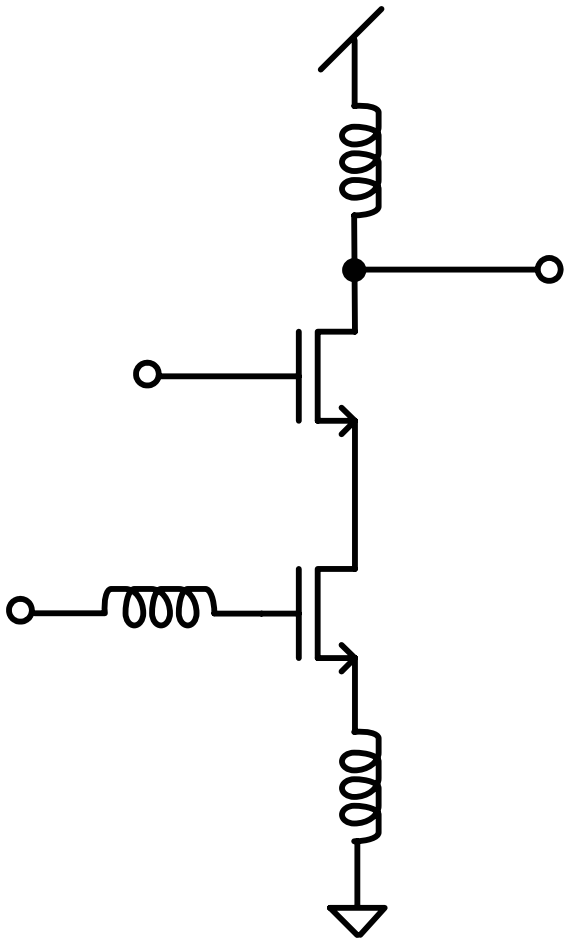
Negative Feedback

- Linearity improvement at the expense of circuit gain
- Second order non-linearity effect on IIP3
- $g_{m3}<0$, leads to further deterioration
- Feedback techniques not suitable at RF frequencies

Negative Feedback

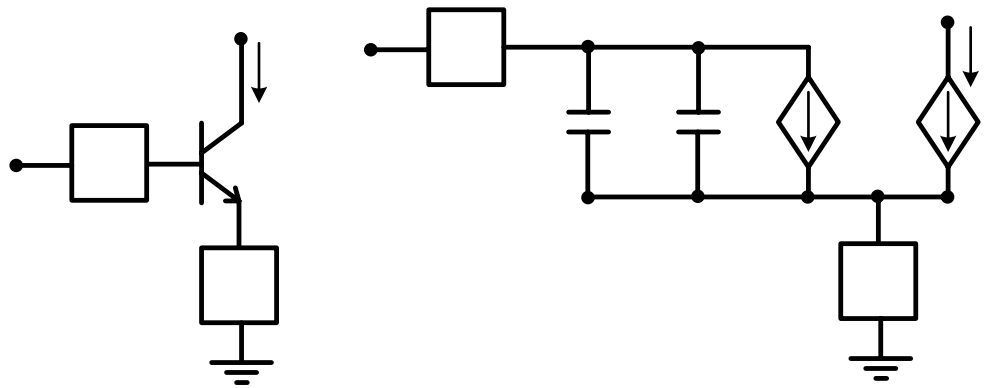
- Inductor L_S acts as a feedback network
- Provides best gain and noise performance
- Poor linearity performance due to second order non-linearity feedback

Cascode LNA



Input Impedance Termination

- Feedback network is frequency dependent
- Different effect on different harmonics



$$|IIP3| \approx \left|\frac{A_1(s)}{I_Q}\right|^3 \left|\frac{V_T}{4}\left[1+sC_{je}Z(s)\right]\left\{-1+\frac{A_1(\Delta s)}{g_m}\left[1+\Delta sC_{je}Z(\Delta s)\right]+\frac{A_1(2s)}{2g_m}\left[1+2sC_{je}Z(2s)\right]\right\}\right| |V_s|^2$$

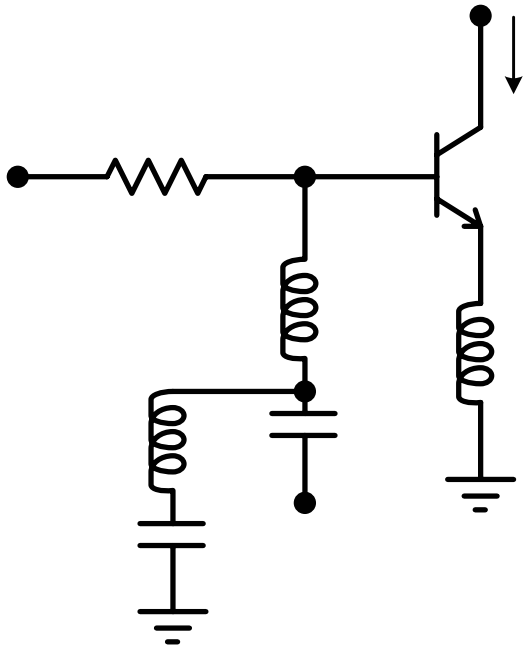
where

$$\Delta s = (s_a - s_b) << s, \quad s_a = j2\pi f_a, \quad s_b = j2\pi f_b$$

$$A_1(s) = \frac{g_m}{sC_{je}Z(s) + s\tau_F g_m Z(s) + g_m \, Z(s)/\beta_o + 1 + g_m Z_e(s)}, \quad Z(s) = Z_b(s) + Z_e(s)$$

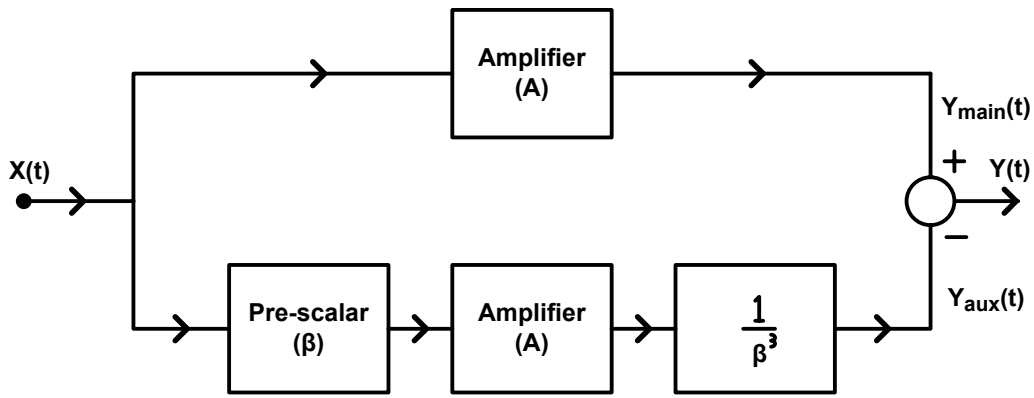
Input Impedance Termination

- The input and output impedances selectively tuned for second harmonic frequencies
- Requires huge passive elements



Feedforward

- Scaled versions of the input signal are fed to two different amplifiers



$$y_{main}(t) = A.x.(1+\alpha_2 x^2), \quad y_{aux}(t) = A.\beta.x.(1+\alpha_2\beta^2 x^2) * \frac{1}{\beta^3}$$

$$y(t) = y_{main}(t) - y_{aux}(t)$$

$$= A\left(1 - \frac{1}{\beta^2}\right).x$$

Feedforward-1

- Drawbacks
  - Linearity improvement at the expense of gain
  - Reduced NF due to additional active components
  - Mismatch and errors in signal scaling leads to reduced improvement
- Derivative Superposition (DS) method addresses the above problems

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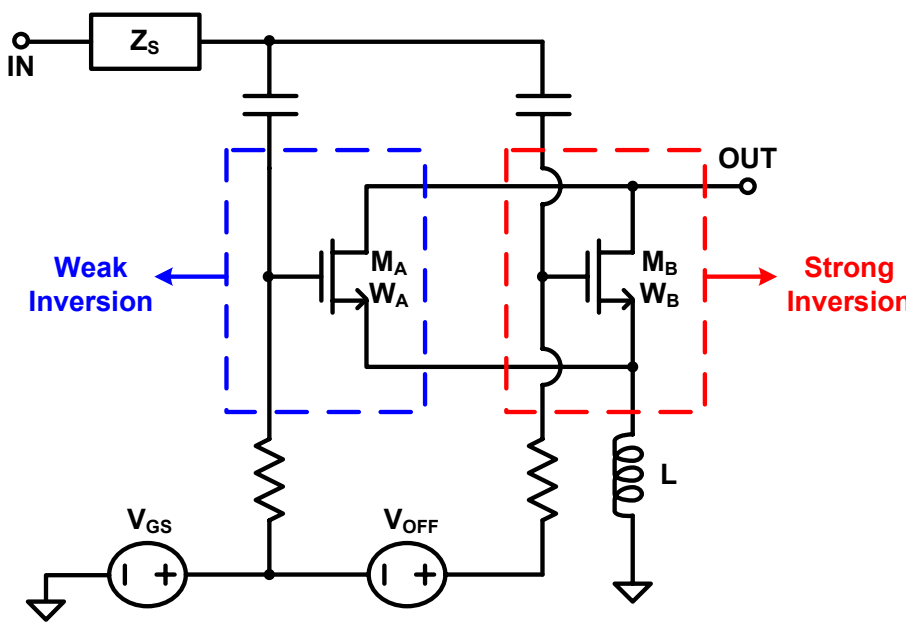
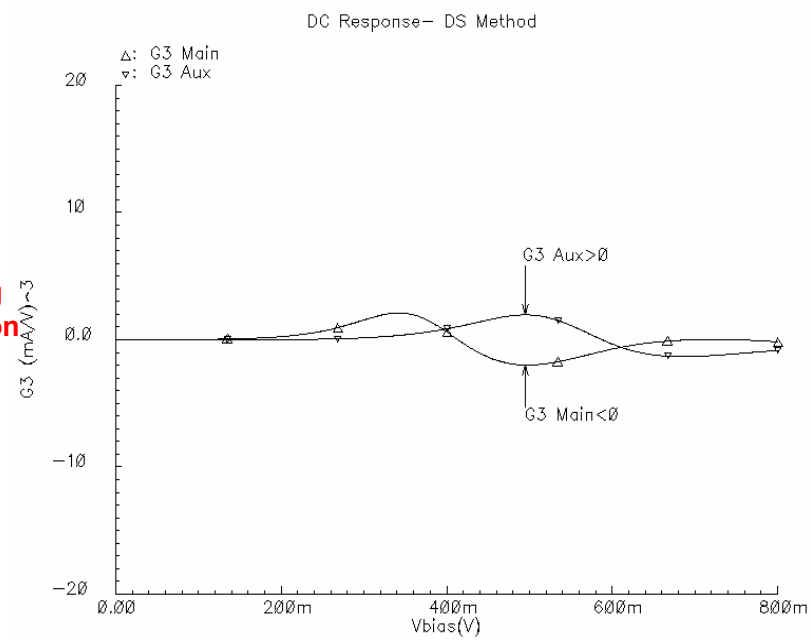
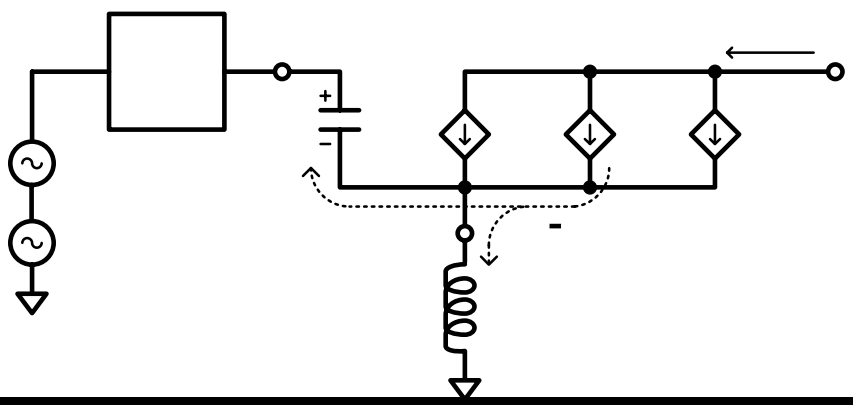
- DS method also addresses the problem of narrow range with optimum biasing technique.
- g_{m3} negative in strong inversion and positive in weak inversion





DS-Method

- Wide range of bias values with very small g_{m3} and hence IIP3 improvement obtained
- Drawbacks
  - Second order harmonics ($2\omega_a, 2\omega_b, \pm\omega_b \pm \omega_a$) converted to voltage at the source
  - Control parameter V_{gs} has both fundamental and second harmonics

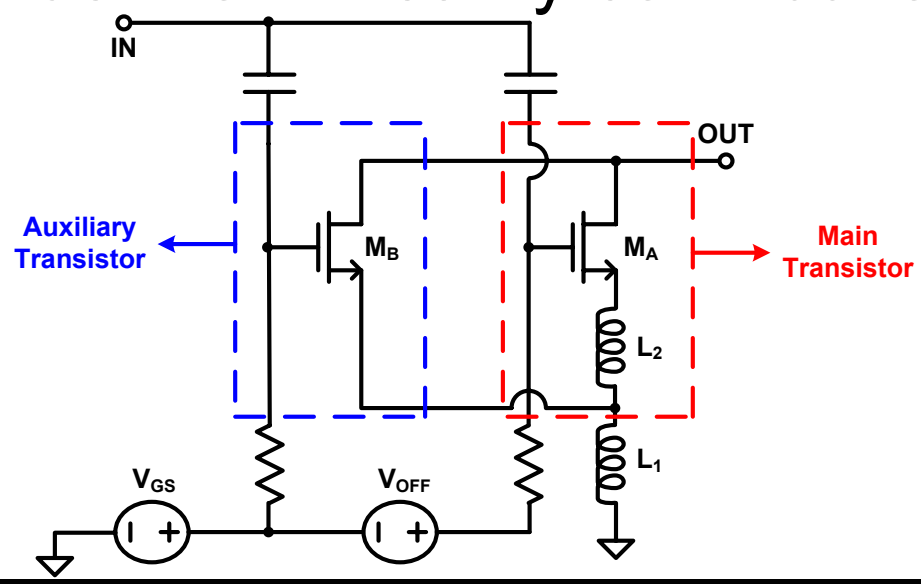


$$IIP3 = \frac{4 g_{m1}^2 \omega^2 L C_{gs}}{3|\varepsilon|}, \text{ Where}$$

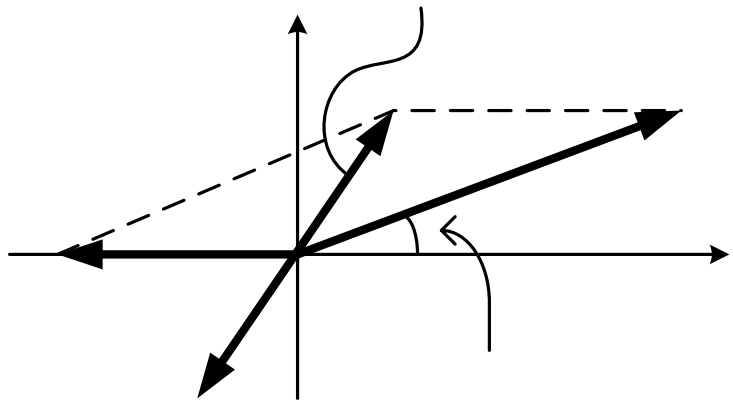
$$\varepsilon = g_{m3} - \frac{2 g_{m2}^2 / 3}{g_{m1} + \frac{1}{2 j \omega L} + 2 j \omega C_{gs} + Z_s(2\omega) \frac{C_{gs}}{L}}$$

Modified DS-Method

- Addresses the effect of second order non-linearity feedback
- Magnitude and phase of second order non-linearity contribution to IM3 is tuned to cancel the third order non-linearity contribution to IM3



Modified DS-Method



$$IIP_3 = \frac{4g_{1A}^2\omega^2\left[L_1\left(C_A + C_B\right) + L_2C_A\right]}{3|\varepsilon|}, \text{ Where}$$

$$\varepsilon = g_{3B}n(s)|n(s)|^2\left[1 + \frac{L_2C_A}{L_1\left(C_A + C_B\right) + L_2C_A}\right] + g_{3A} - \frac{2g_{2A}^2}{3g_{1A}}\frac{1}{1 + \frac{1}{j2\omega(L_1 + L_2)g_{1A}}}$$

$$n(s) = 1 + j\omega L_2 g_{1A}$$

Drawbacks

- Weak inversion transistor connected in parallel degrades NF

$$i_{nd}^2 = 4kT\Delta f \gamma g_{d0}$$

$$i_{ng}^2 = 4kT\Delta f \delta \frac{\omega^2 C_{gs}^2}{5 g_{d0}}$$

$$g_{d0} = I_{Dsat} / \phi_t$$

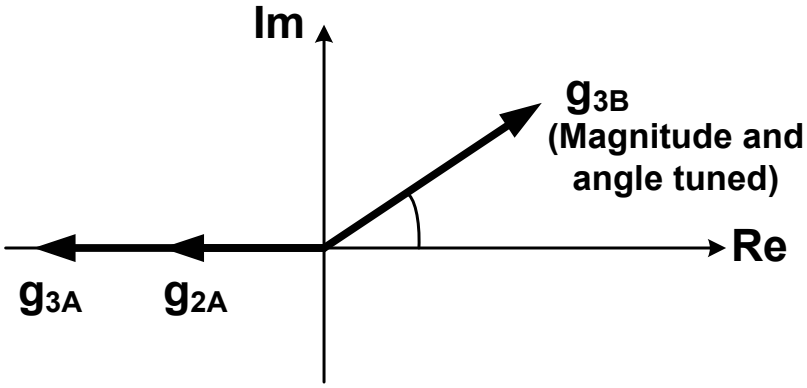
- Auxiliary transistor loads the input affecting the frequency of operation
- Auxiliary transistor affects both linearity and input match leading to increased design steps

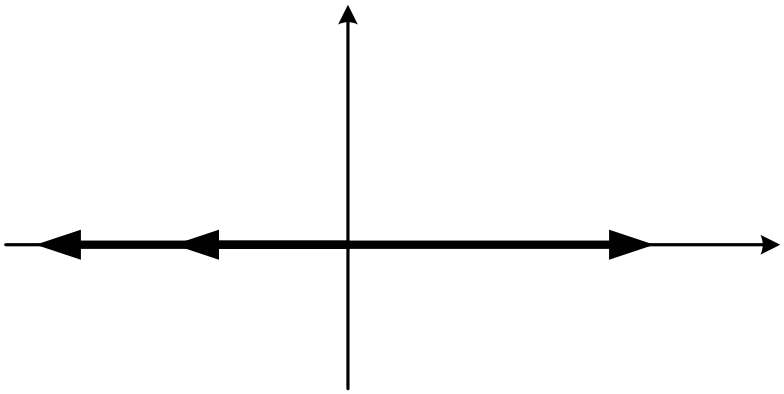
Proposed Solution

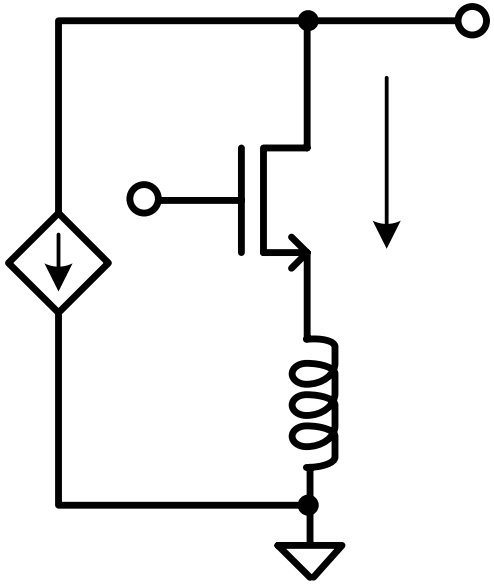
Basic Idea

- An auxiliary circuit is unavoidable to achieve high linearity
- IM3 components in the drain current of the main transistor has the required information of its non-linearity
- Auxiliary circuit is used to tune the magnitude and phase of IM3 components
- Addition of main and auxiliary transistor currents results in negligible IM3 components at output

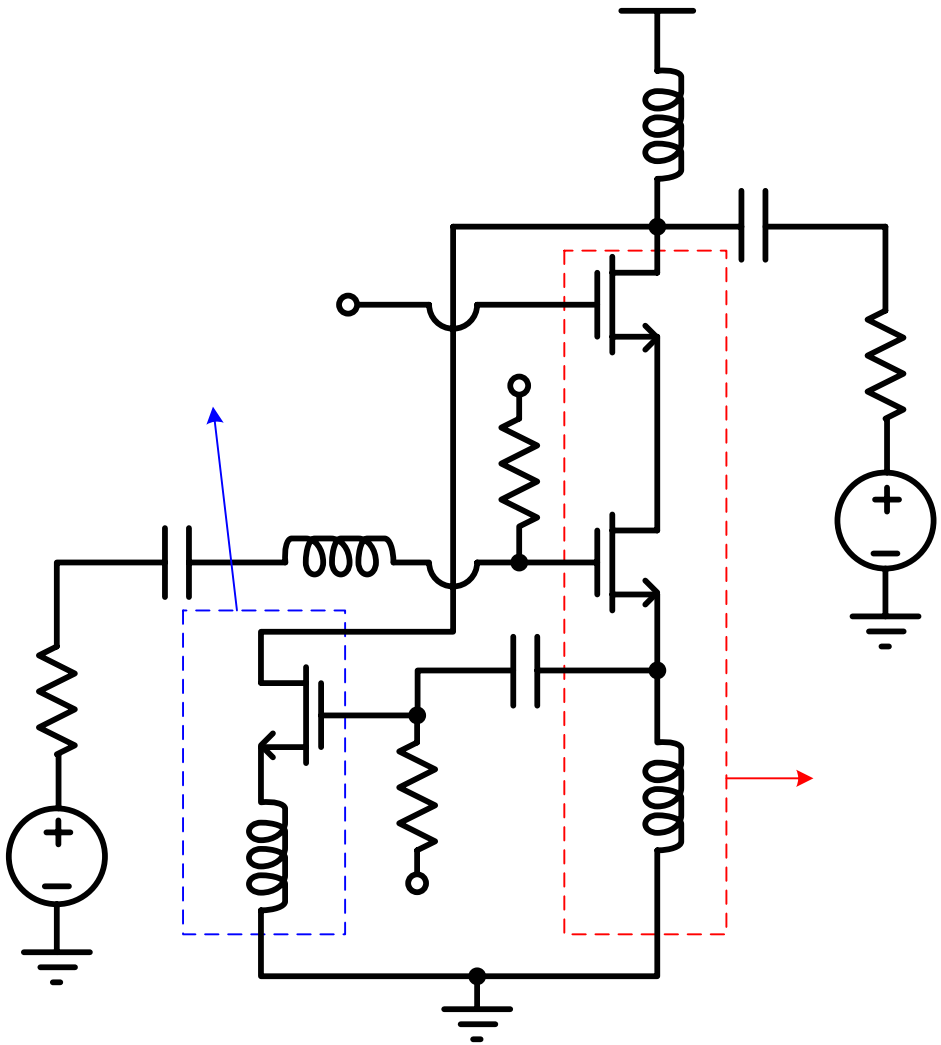
Basic Idea





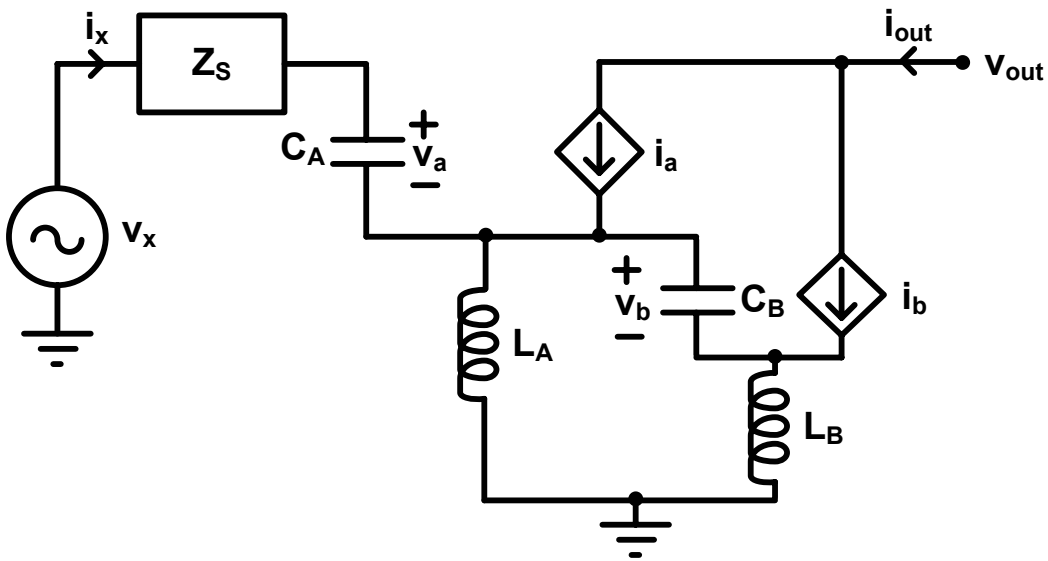


Proposed LNA



Theoretical Analysis

- IIP3 derived using the harmonic input method of Volterra series analysis



$$i_a = g_{1a} v_a + g_{2a} v_a^2 + g_{3a} v_a^3$$

$$i_b = g_{3b} v_b^3$$

$$i_{out} = i_a + i_b = C_1(s_1) * v_x + C_2(s_1, s_2) * v_x^2 + C_3(s_1, s_2, s_3) * v_x^3$$

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Theoretical Analysis

$$IIP3 = \frac{1}{6\,\mathrm{Re}\left(Z_s(s)\right)\left|A_1(s)\right|^2}\left\{\frac{g_{1a}}{\varepsilon}\right\}$$

$$where,\ \varepsilon = g_{3a} - \frac{g_{2a}^2}{3g_{1a}} + g_{3b}n(s)\left|n(s)\right|^2 \frac{2+s^2L_BC_B}{2(1+s^2L_BC_B)}$$

$$n(s) = \frac{sL_A(g_{1a}+sC_A)}{1+sC_B(sL_A+sL_B)}$$

- The effect of second order non-linearity can be seen in the above equation
- The value of g_{3b} can be tuned to obtain high IIP3 by choosing appropriate values for the inductors L_A and L_B and the aspect ratios of the transistors.

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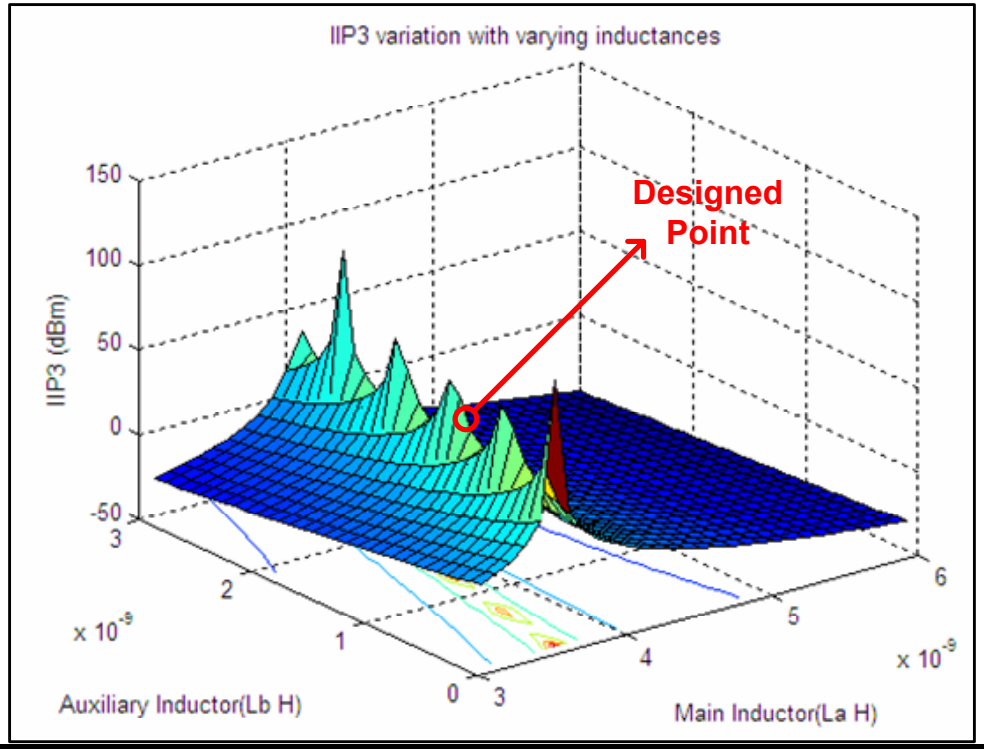
Theoretical Analysis

- MATLAB plots for different values of L_A and L_B is plotted
- The result corroborates the idea of IIP3 improvement by cancellation of IM3 components



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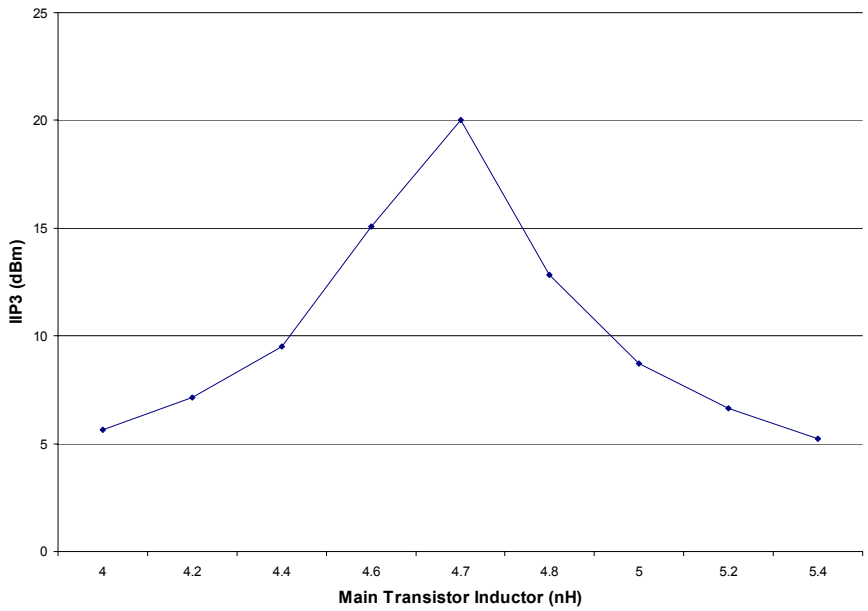
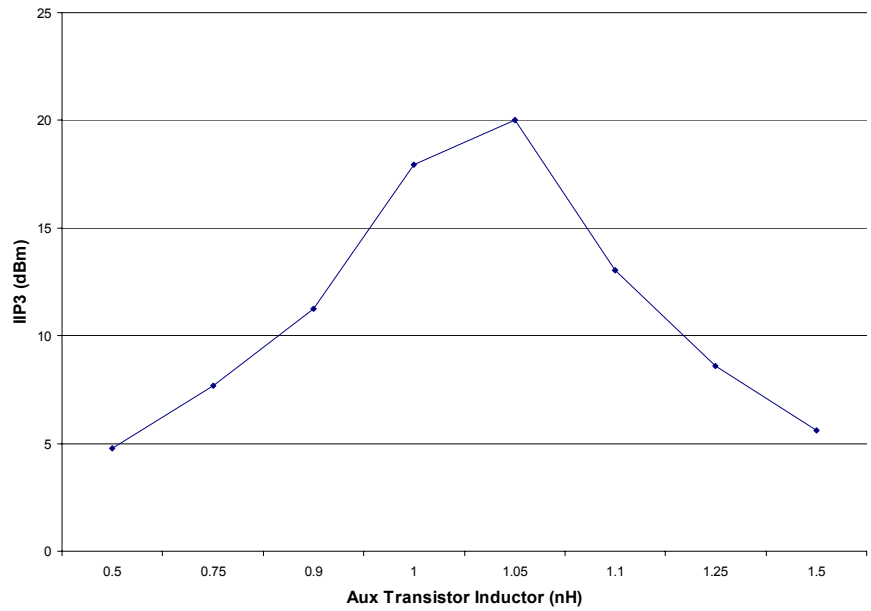
IIP3 Sensitivity

Variation with La



Variation with Lb



Effect on Input Match

- If $\left|s^2 L_A C_B\right| << 1$, the input impedance can be simplified to that of a cascode LNA

$$Z_{in} = sL_G + \frac{1}{sC_A} + sL_A + \frac{g_{1a} L_A}{C_A}$$

- The input matching is unaffected by the auxiliary transistor

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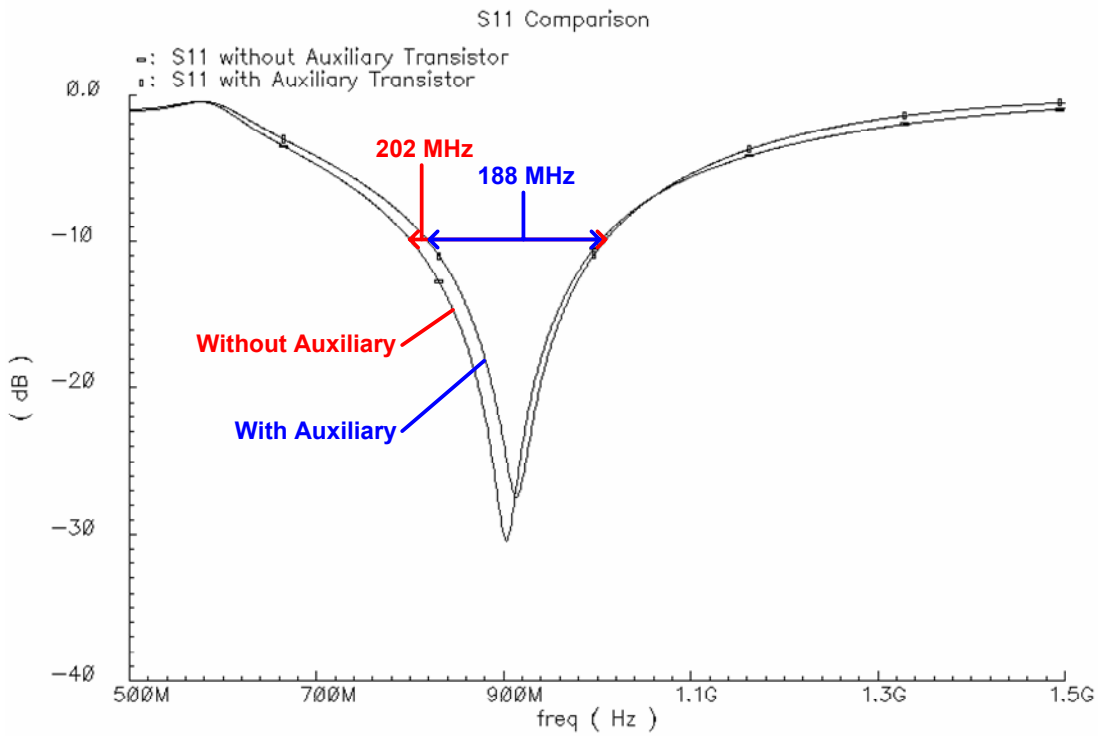
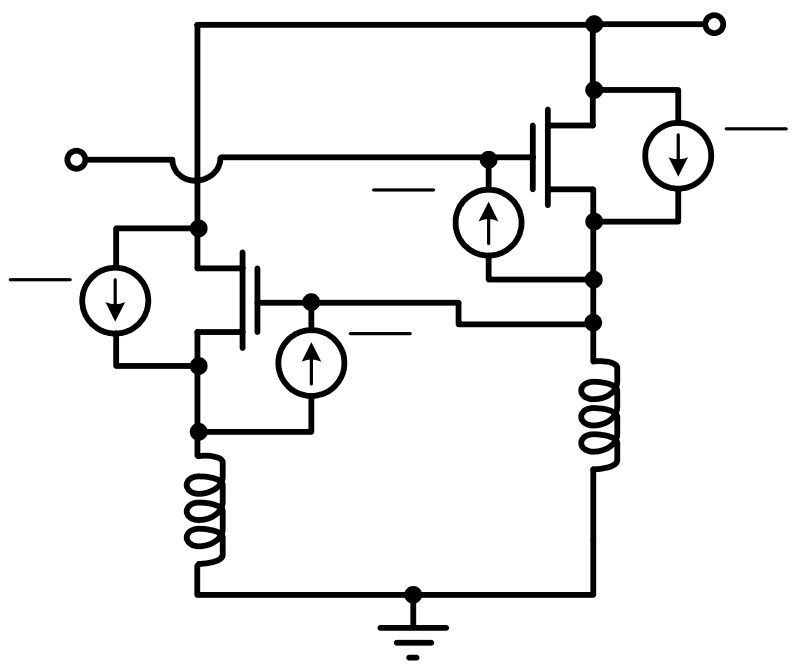
Effect on Input Match

- Effect on input match (S_{11}) with and without auxiliary transistor



Effect on NF

- The gate noise current of the auxiliary transistor gets added with the drain noise current of main transistor and is attenuated by the gain of LNA



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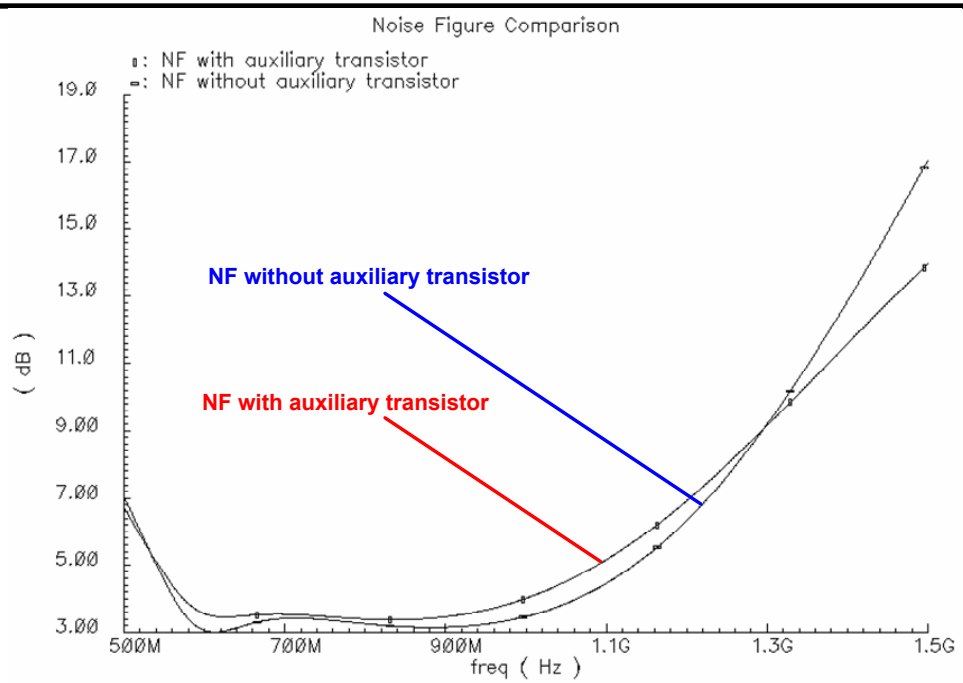
Effect on NF



- 0.3dB degradation in NF observed
- Lossy inductor in the auxiliary branch contributes to increased NF

LNA Design

- Linear LNA was designed and fabricated in TSMC 0.35μm CMOS technology
- The inductors were designed using ASITIC and a Q of 2.5 was obtained
- The LNA was designed to have maximum gain at 900MHz
- The LNA fabricated was a stand alone LNA terminated by the 50Ω port impedance

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Component Values

Component	Value
M_A	24 μm/0.4 μm, m=16
M_C	24 μm/0.4 μm, m=16
M_B	24 μm/0.4 μm, m=36
L_G	30 nH
L_A	5 nH
L_B	1.05 nH
L_D	10 nH

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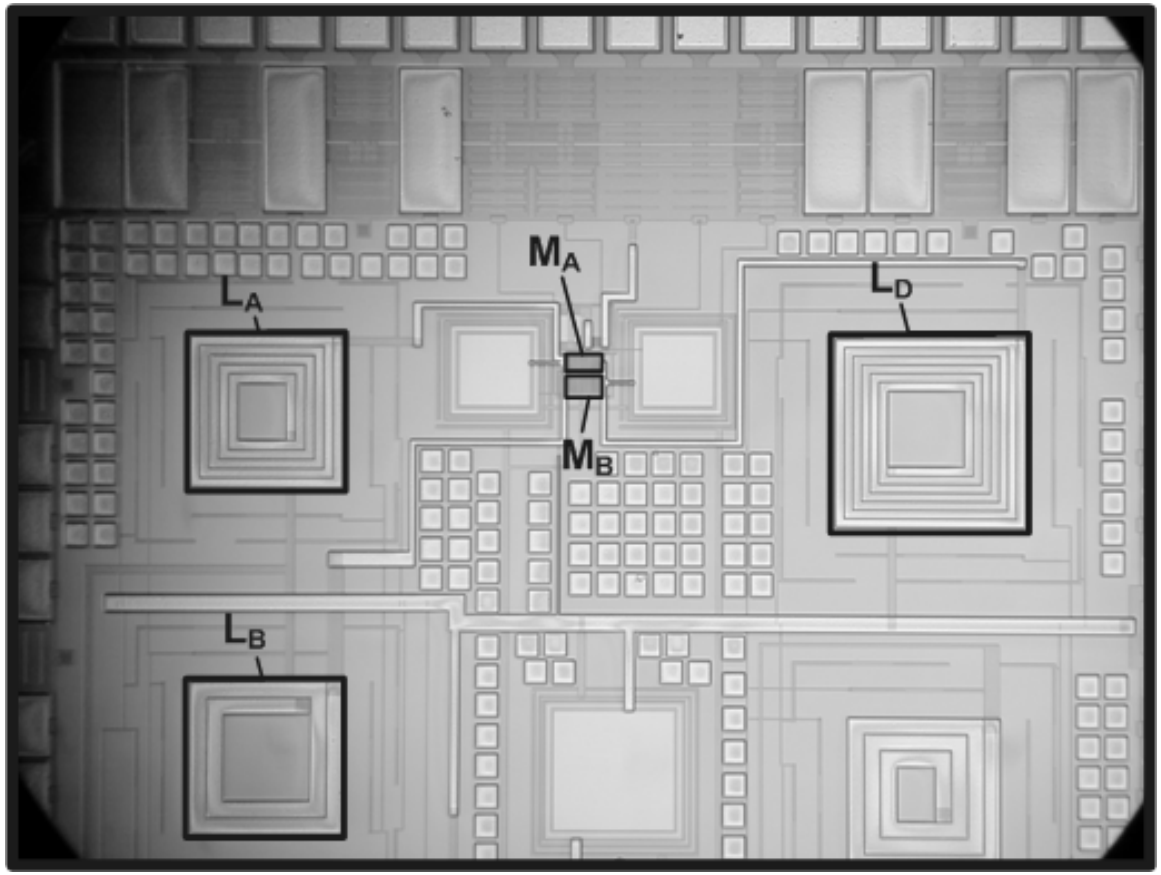
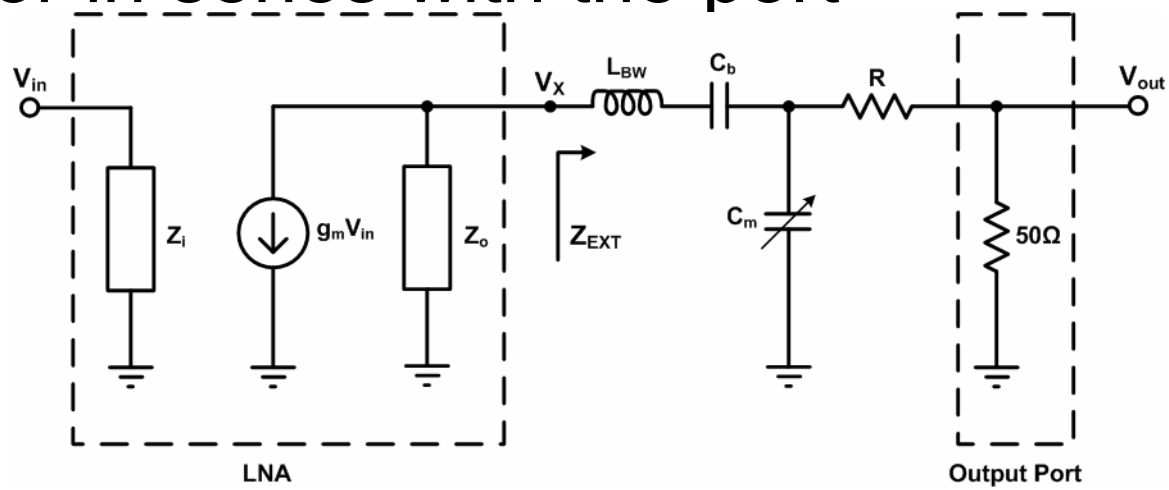
Chip Photograph



Testing Strategy

- The gain obtained in LNA is less as it sees a 50Ω load impedance
- Gain can be improved by connecting a resistor in series with the port



•LNA Gain= $\frac{V_x}{V_{in}} = \frac{V_{out}}{V_{in}} * \frac{R+50}{50}$

Advantages

- Increased gain results in larger signal swings
- LNA subject to large signal swings is an ideal test for linearity
- Linearity of LNA unaffected due to linear resistive element

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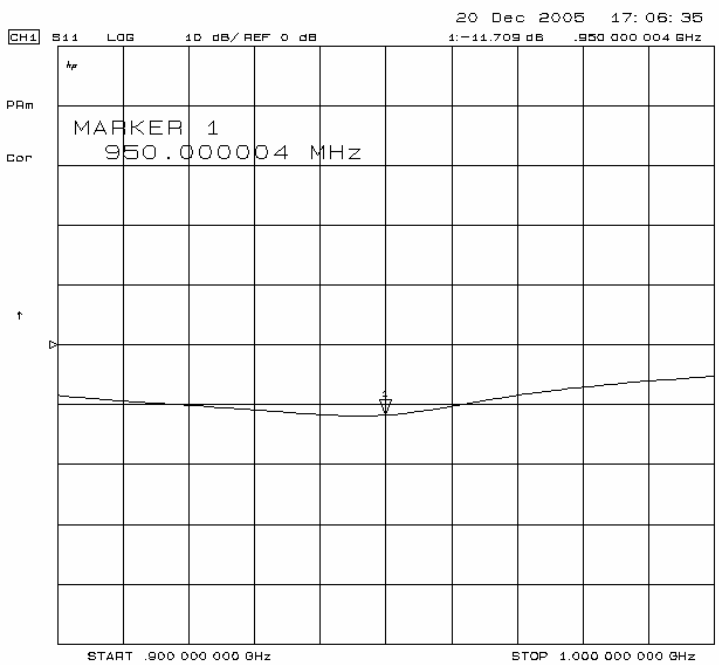
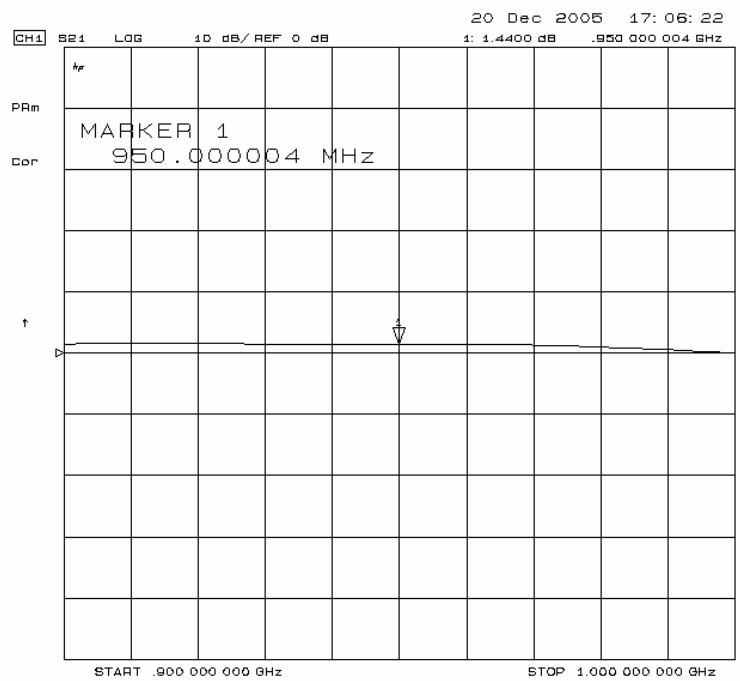
Experimental Results

- R=0Ω, S_{11}=-15.85 dB, S_{21}=4.4 dB, Gain= 4.4 dB

S_{11} (Input Match)	S_{21} (Power Gain)
	

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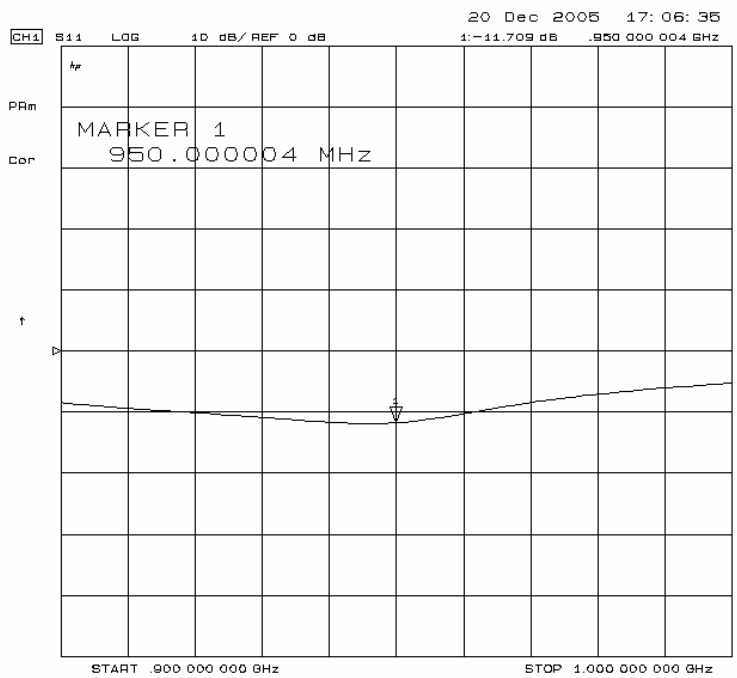
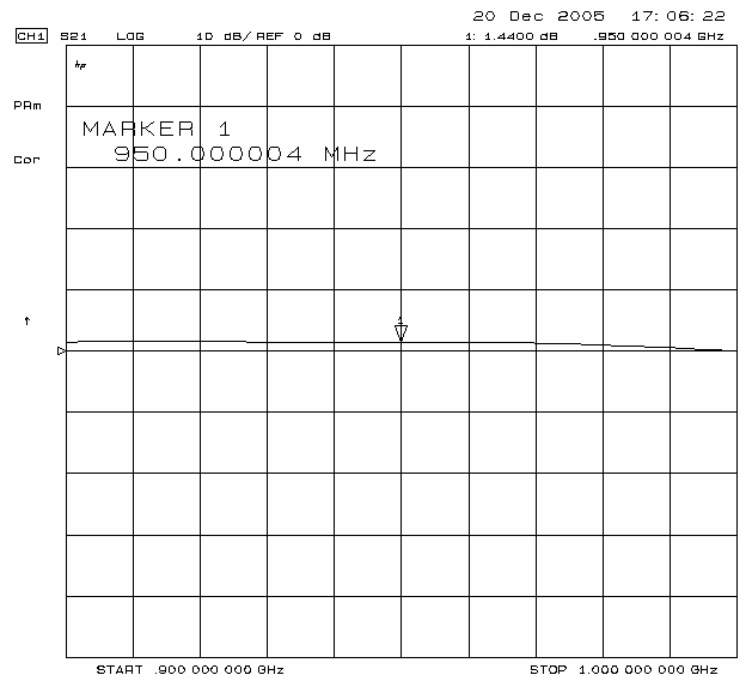
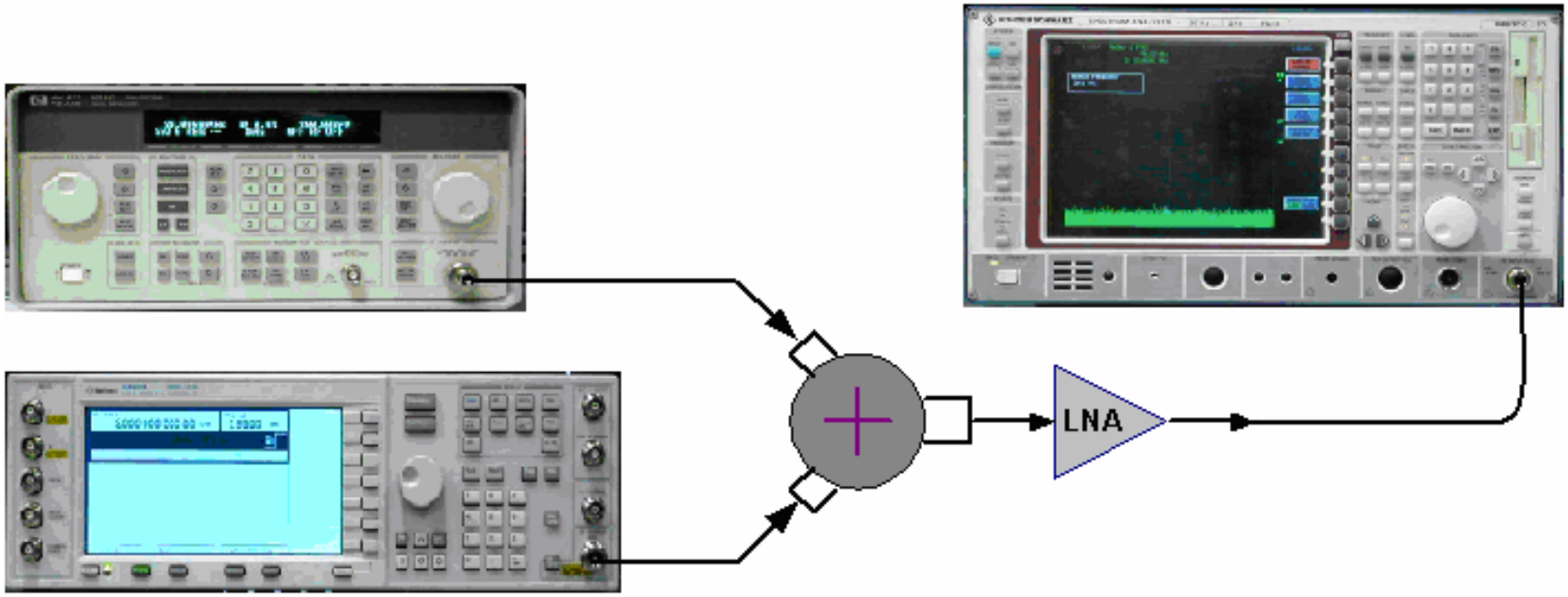
Experimental Results

- R=75 Ω, S_{11}=-11.7 dB, S_{21}=1.5 dB, Gain= 9.5 dB

S_{11} (Input Match)	S_{21} (Power Gain)
	

IIP3 Test Setup



IIP3 Measurement

- R=75 Ω

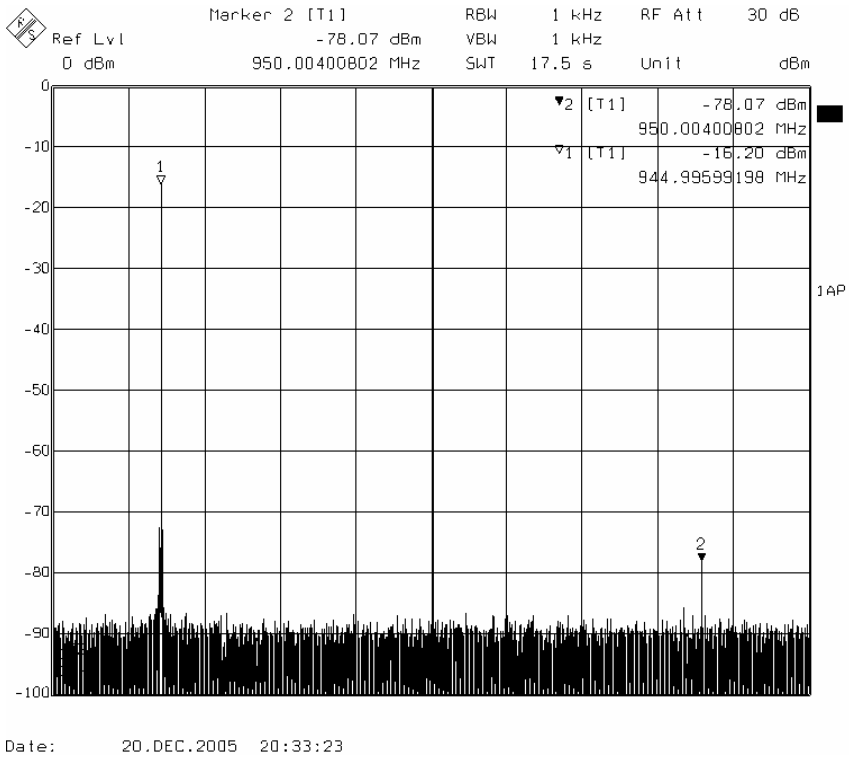
$$IIP3(dBm) = P_{in} + \frac{P_f - P_{IM3}}{2}$$

$$\text{where } P_{in} = \text{Total Signal Input Power}$$

$$P_f = \text{Total Signal Output Power}$$

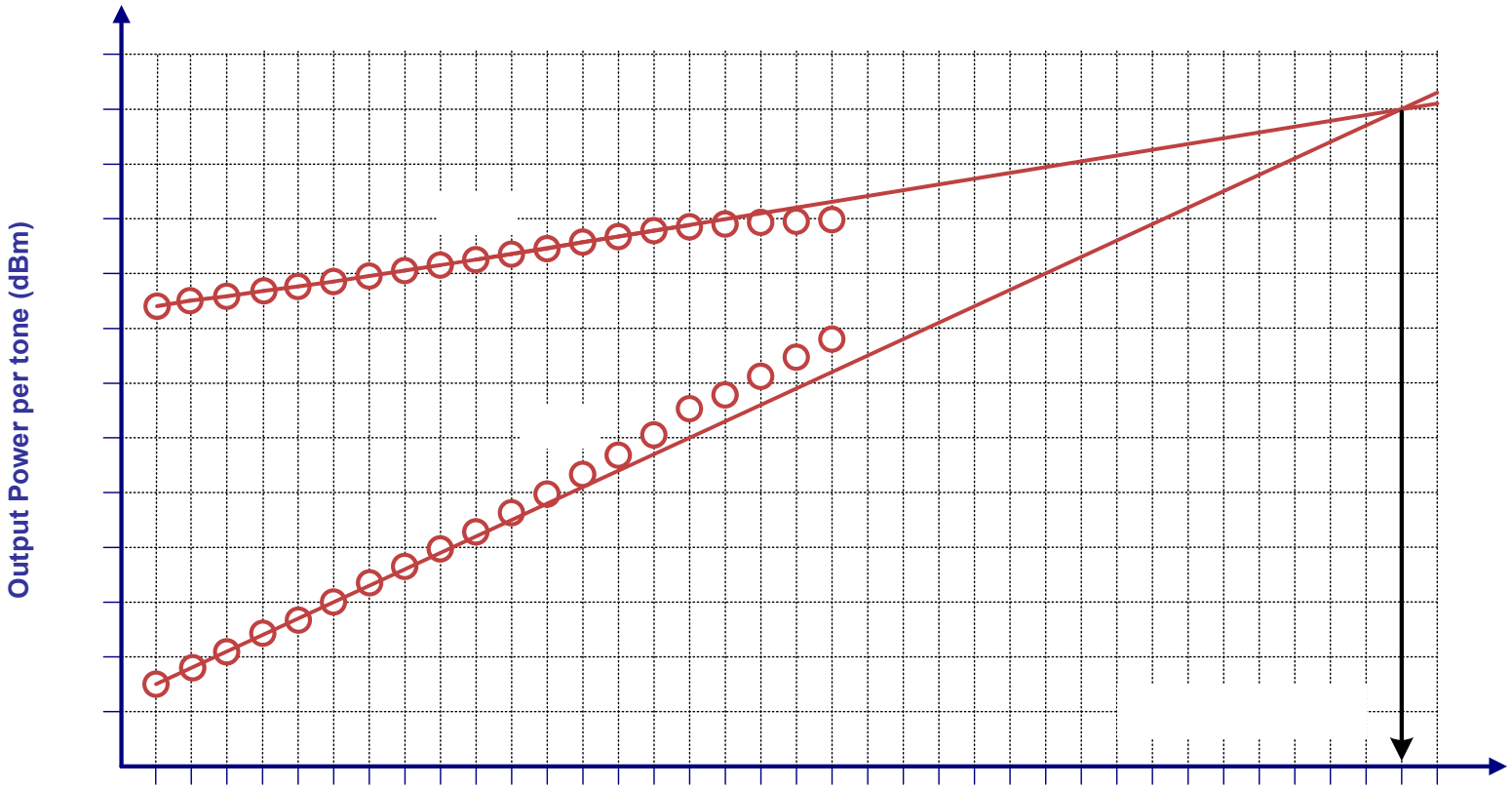
$$P_{IM3} = \text{Total IM3 tone Output Power}$$

- P_{in}=-10dBm, P_f= -13.2dBm
  P_{IM3}= -75.07dBm
- IIP3 = +20.93 dBm



AMSC

IIP3 Measurement

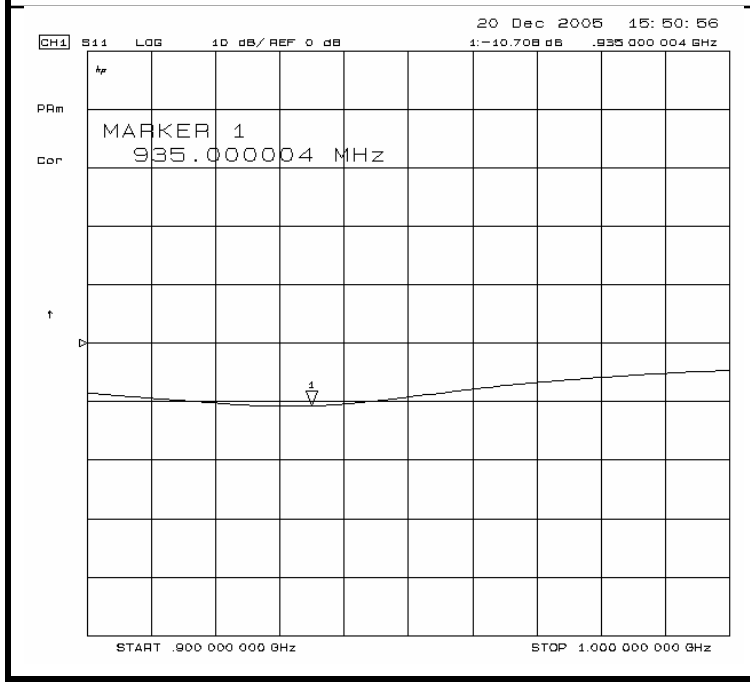


AMSC

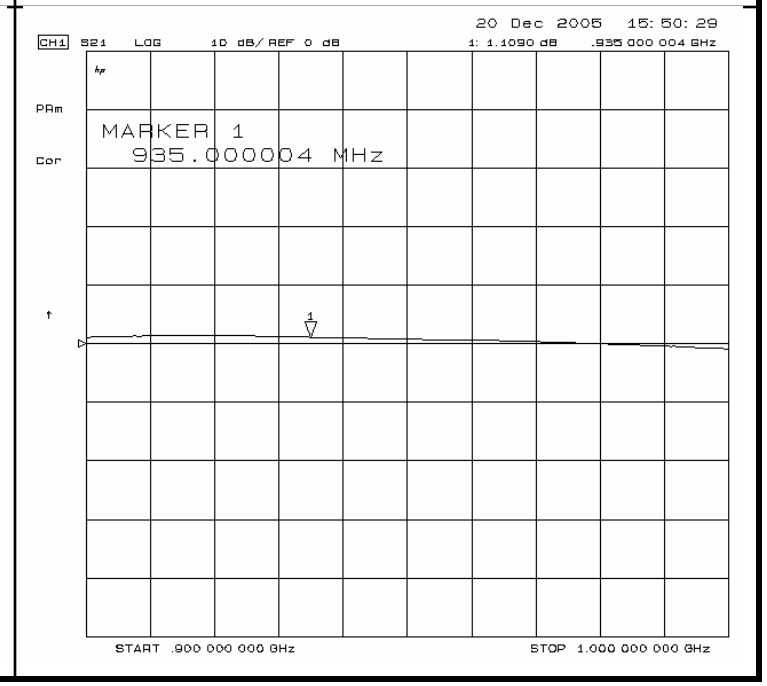
Experimental Results

- R=100 Ω, S_{11}=-10.7 dB, S_{21}=1.1 dB, Gain= 10.6 dB

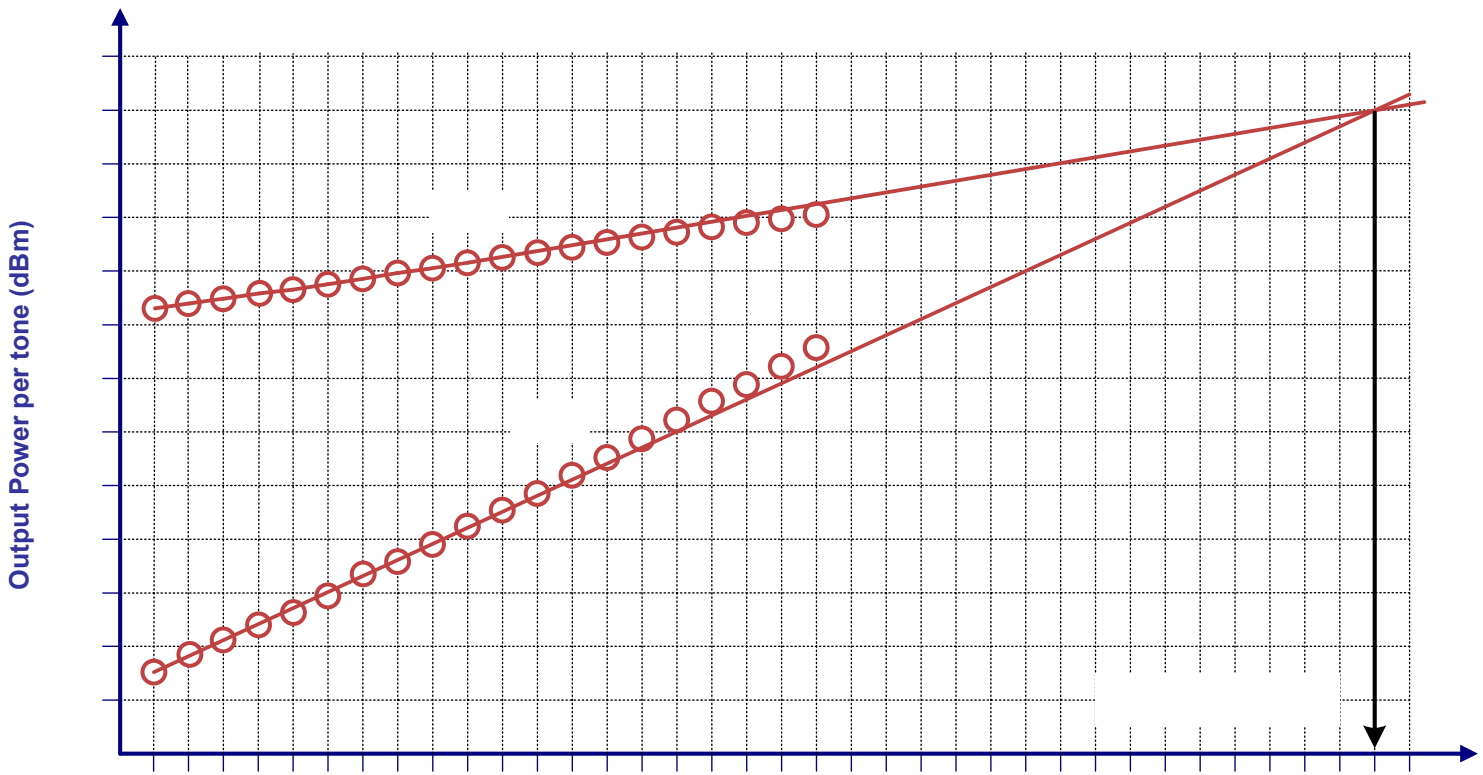
S_{11} (Input Match)



S_{21} (Power Gain)



IIP3 Measurement



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Summary of Results

R (Ω)	S_{11} (dB)	S_{21} (dB)	LNA Gain (dB)	IIP3 (dBm)
0	-15.85	4.4	4.4	20
75	-11.7	1.5	9.5	20.9
100	-10.7	1.1	10.6	21
150	-9.5	-0.5	11.5	20.5

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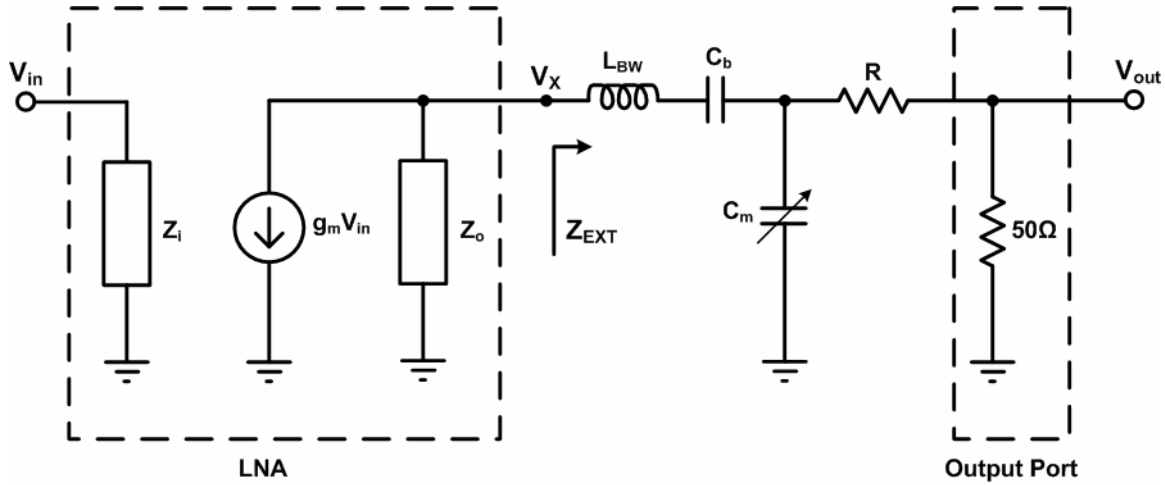
De-embedding Results



- 6dB increment in gain when 'R' is changed from 0Ω to 100Ω and hence on-chip load resistance can be computed to be 150Ω
- Gain of LNA with Zext=∞ is 6dB more than gain with R=100Ω
- Gain of LNA adding other losses is estimated to be 18.5dB
- The NF of the LNA after de-embedding the noise contribution of termination resistors (R=100Ω and 50Ω port) is calculated to be 1.76dB

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Comparison of Results

Work	Technology	Freq (GHz)	Gain (dB)	NF (dB)	IIP3 (dBm)	P_{dc} (mW)	FOM
This Work	0.35μm CMOS	0.95	18.5	1.76	21	22.5	793
JSSC '04	0.35μm CMOS	0.9	10	2.8	15.6	21.1	19
ISSCC '01	0.35μm CMOS	0.9	2.5	2.8	18	45	3
MTT '05	0.25μm CMOS	0.9	15.5	1.65	22	24.2	503
ISCAS '04	0.25μm CMOS	0.9	14.6	1.8	10.5	5.4	117
ESSCC '05	0.5μm SiGe BiCMOS	0.88	15.7	1.4	11.7	11.7	124
ISCAS '04	0.18μm CMOS	3	6.5	1.9	15	8.9	29
ISSCC '03	0.25μm CMOS	2.2	14.9	3	16.1	23.5	54

De-Embedding the NF of LNA

Fig 1 shows the simplified small signal model of LNA. RL is the load impedance of LNA presented by the LC resonant circuit at the output, R is the external resistor connected to improve the gain and 50Ω is the resistance of the port.

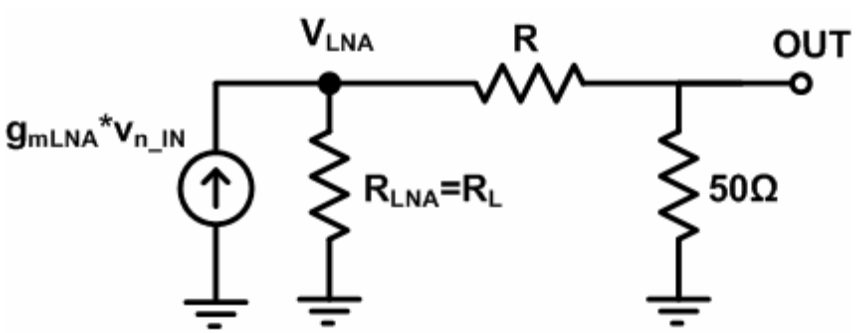

Fig 1: Small Signal Model

For numerical analysis a value of RL=150Ω and R=75Ω are used below.

From Table 3 in the paper, the measured gain at the point VLNA shown in Fig 1 is 10.5dB for R=75Ω and NF is 2.95dB. Hence

$$NF = 1 + \frac{V_{measured-in}^2}{V_{50\Omega}^2} = 10^{2.95/10} = 1.972 \qquad (1)$$

Noise Analysis at output:

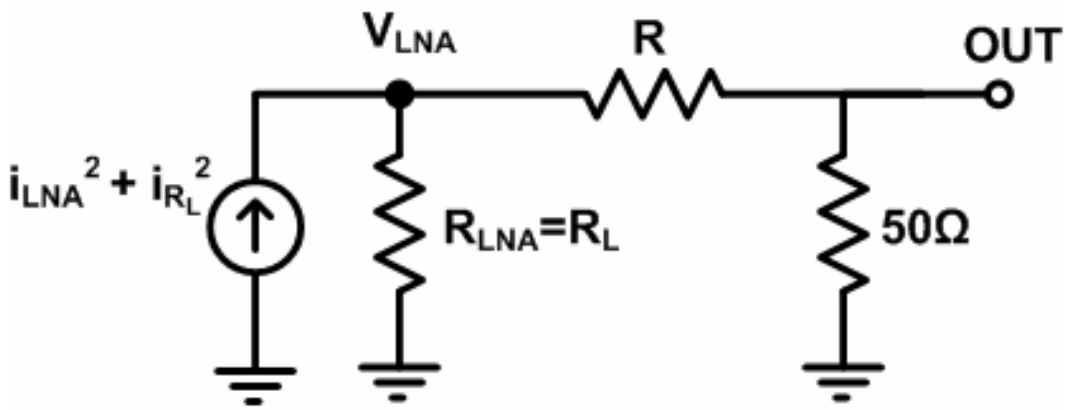

Fig 2: Noise Analysis

Fig 2 shows the model used for noise analysis. i_{LNA}^2 and i_{RL}^2 are the noise currents due to input transistor and the load resistance (R_L) respectively.

$i_{LNA}^2 + i_{RL}^2$ is reflected to the output port to generate $v_{LNA_out}^2$

.

The resistors R and 50Ω generate an output noise voltage at the node 'OUT' given by

$$V_{add}^2 = 4KT\left[\frac{1}{50}\left(\frac{R+R_L}{R+R_L+50}\right)^2 50^2 + R\left(\frac{50}{R+R_L+50}\right)^2\right] \qquad (2)$$

$$= 4KT*50\left[\left(\frac{R+R_L}{R+R_L+50}\right)^2 + \frac{R*50}{(R+R_L+50)^2}\right]$$

$$= 4KT*50*(0.72)$$

The output noise measured at the node 'OUT' is the sum of noise contributed by the LNA and the output resistive network formed by R and 50Ω and is given as follows.

$$V_{measured-out}^2 = V_{LNA_out}^2 * \left(\frac{50}{R+50}\right)^2 + V_{add}^2 \qquad (3)$$

$$= V_{LNA_out}^2 * \left(\frac{50}{R+50}\right)^2 + 4KT * 50 * 0.72 \quad (from\ (2))$$

The overall gain of LNA for R=75Ω is given as follows.

$$Overall\ \ Gain = \frac{V_{out}}{V_{in}} = \frac{V_{LNA_out}}{V_{in}} * \frac{V_{out}}{V_{LNA_out}}$$

$$\frac{V_{LNA_out}}{V_{in}} = 10.5\,dB = 3.35$$

$$\frac{V_{out}}{V_{LNA_out}} = \frac{50}{50+75} = 0.4$$

$$Overall\ \ Gain(A_v) = 3.35 * 0.4 = 1.34$$

Total input measured noise is given as follows.

$$V_{measured-in}^2 = \frac{V_{measured-out}^2}{A_v^2}$$

$$= V_{LNA-in}^2 + \frac{4KT*50*0.72}{A_v^2} \qquad (from\ (3))$$

Where V_{LNA-in}^2 is the total input referred noise contribution of LNA and R_L alone.

$Let\ V_{n50}^2 = 4KT*50$ Hence total input referred noise contribution of LNA and the load resistor alone is given by

$$V_{LNA-in}^2 = V_{n50}^2\left[10^{2.95/10} - 1\right] - \frac{V_{n50}^2 * 0.72}{A_v^2} \qquad (from\ (1))$$

$$= V_{n50}^2(0.9 - 0.4)$$

$$= V_{n50}^2(0.5)$$

De-embedded NF = 1+0.5=**1.76dB**

Conclusion

- A highly Linear LNA using a non-linearity cancellation technique has been proposed
- Theoretical analysis using Volterra series has been done to corroborate the idea
- The LNA has been designed and fabricated in TSMC 0.35μm technology
- An IIP3 of +21dBm has been experimentally achieved