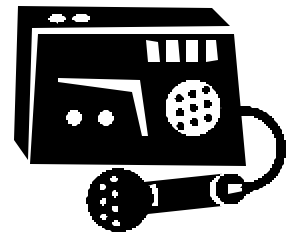




Low Noise Amplifier

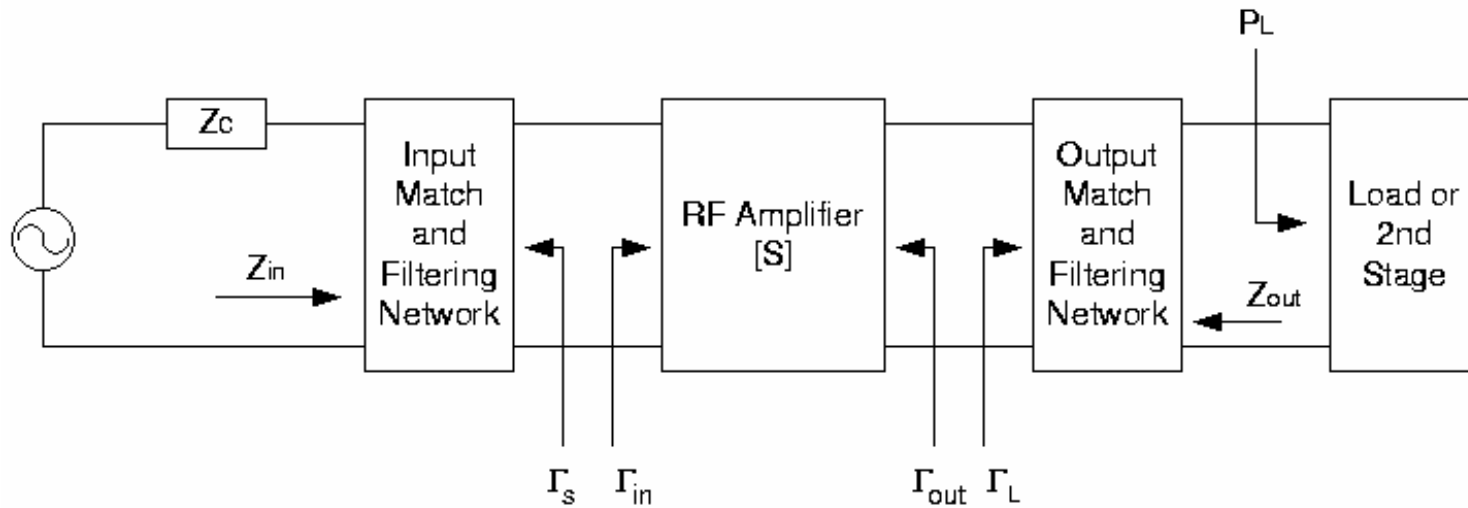


The material here provided is mainly based on Dr. Chunyu Xin's dissertation at TAMU

Overall Requirements of LNA in Receivers

- ❑ Signal coming from antenna is very small: -100dBm ($3.2\mu\text{V}$) ~ -70dBm (0.1mV), amplification is need for the following stage (mixer) to handle. (Gain requirement)
- ❑ The received signal should have certain SNR to be reliable detected. Noise comes from the environment and the circuit itself. Noise floor is determined by thermal noise and system bandwidth (KTB). Noise added by the circuit should be as less as possible. (Noise requirement).
- ❑ Large signal or blocker can occur at the input of LNA. Large signal performance of LNA should be good enough. (Linearity requirement)
- ❑ Reasonable power consuming (Power constrain)

A Conceptual LNA Structure



LNA consists of:

- ❑ Input/output match network
- ❑ Amplifier transistor (s)
- ❑ Power source
- ❑ Load

Important terms:

Source reflection coefficient: Γ_s

Load reflection coefficient: Γ_L

Input reflection coefficient:

$$\Gamma_{in} = s_{11} + \frac{s_{12}s_{21}\Gamma_L}{1 - s_{22}\Gamma_L}$$

Amplifier S matrix:

$$[S] = \begin{pmatrix} s_{11} & s_{21} \\ s_{12} & s_{22} \end{pmatrix}$$

Output reflection coefficient:

$$\Gamma_{out} = s_{22} + \frac{s_{12}s_{21}\Gamma_s}{1 - s_{11}\Gamma_s}$$

LNA Metrics: Gain

- Gain is the ratio of output signal and input signal. It defines and small signal amplification capability of LNA.
- A lot of gain definitions exist. For IC implementation, LNA input is interfaced off-chip and usually matched to specific impedance (50ohm or 75ohm). Its output is not necessary matched if directly drive the on-chip block such as mixer. This is characterized by voltage gain or transducer power gain by knowing the load impedance level.
- Transducer power gain: Power delivered to the load divided by power available from source.

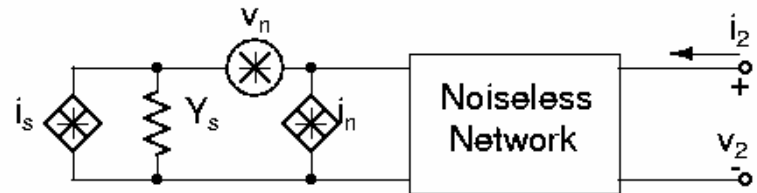
$$G_T = \frac{1 - |\Gamma_s|^2}{|1 - s_{11}\Gamma_s|^2} |s_{21}|^2 \frac{1 - |\Gamma_L|^2}{|1 - s_{22}\Gamma_L|^2} \quad \text{For unilateral device} \\ \text{i.e. } S_{12} \sim 0$$

LNA Metrics: Noise Figure

- ❑ Noise factor is defined by the ratio of output SNR and input SNR. Noise figure is the dB form of noise factor.
- ❑ Noise figure shows the degradation of signal's SNR due to the circuits that the signal passes.

$$F = \frac{SNR_i}{SNR_o} \quad NF(dB) = 10 \log F$$

$$F = F_{\min} + \frac{R_n}{G_s} |Y_s - Y_{opt}|^2$$



LNA noise matching:

The source impedance $1/Y_s$ of the LNA can be transformed to an optimal value such that the noise figure is minimum.

LNA Metrics: Why gain and low noise?

$$Sensitivity = \underbrace{Noise\ floor\ (dBm) + SNR + NF_{tot}}_{-174dBm+10\log BW}$$

System SNR is determined by BER requirement of a specific modulation scheme:

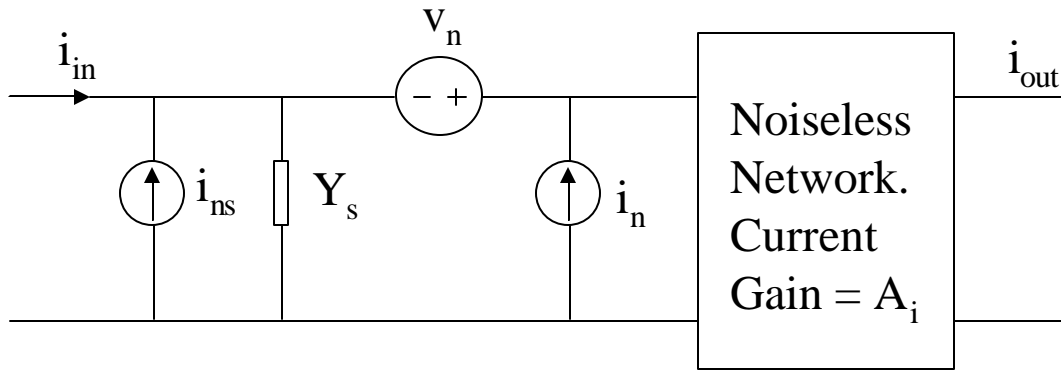
	1e-3	1e-6
QPSK	7dB	11dB
16QAM	12dB	16dB
64QAM	17dB	21dB

Noise factor of cascaded system:

$$F_{tot} = F_{LNA} + \frac{F_{afterLNA} - 1}{G_{LNA}}$$

- ❑ LNA's noise factor directly appears in the total noise factor of the system.
- ❑ LNA's gain suppress the noise coming from following stages

TWO-PORT NOISE COMPONENTS



$$N_{o,total2} = i_{ns}^2 + |i_n + Y_s v_n|^2 \quad ; \quad N_{o,source} = i_{ns}^2$$

$$F = \frac{N_{o,total}}{N_{o,source}} = 1 + \frac{|i_n + Y_s v_n|^2}{i_{ns}^2}$$

where i_n and v_n are partially correlated

$$i_n = i_c + i_u \quad ; \quad i_c = Y_c v_c$$

$$v_n = v_c + v_u$$

Then

$$F = 1 + \frac{i_u^2 + |Y_c + Y_s|^2 v_c^2 + v_u^2 |Y_s|^2}{i_{ns}^2} = 1 + \frac{i_u^2 + |Y_c + Y_s|^2 v_n^2}{i_{ns}^2}$$

$$F = 1 + \frac{\frac{i_n^2}{4kTB} + |Y_c + Y_s|^2 \frac{v_c^2}{4kTB} + \frac{v_u^2}{4kTB} |Y_s|^2}{\frac{i_{ns}^2}{4kTB}}$$

$$F = 1 + \frac{G_u + |Y_c + Y_s|^2 R_c + R_u |Y_s|^2}{G_s} = 1 + \frac{G_u + |Y_c + Y_s|^2 R_n}{G_s}$$

where

$$G_u = \frac{i_u^2}{4kTB} \quad , \quad R_c = \frac{v_c^2}{4kTB}$$

$$R_u = \frac{v_u^2}{4kTB} \quad , \quad G_s = \frac{i_{ns}^2}{4kTB}$$

and

$$R_n = \frac{v_n^2}{4kTB}$$

$Y_{c,s} = G_{c,s} + jB_{c,s}$, then

$$F = 1 + \frac{G_u + [(G_c + G_s)^2 + (B_c + B_s)^2]R_c + (G_s^2 + B_s^2)R_u}{G_s}$$

Optimal source admittance:

Now if

$$\frac{\partial F}{\partial G_s} = 0 \quad \text{and} \quad \frac{\partial F}{\partial B_s} = 0$$

$$B_{opt} = -B_c = B_s$$

$$G_{opt} = G_s = \sqrt{\frac{G_u}{R_n} + G_c^2}$$

then

$$F_{min} = 1 + 2R_n[G_{opt} + G_c] = 1 + 2R_n \left[\left(\frac{G_u}{R_n} + G_c^2 \right)^{1/2} + G_c \right]$$

$$F = F_{min} + \frac{R_n}{G_s} \left[(G_s - G_{opt})^2 + (B_s - B_{opt})^2 \right]$$

For the MOSFET noise model, we have to take into account two sources.

$$\overline{i_{nd}^2} = 4kT\gamma g_{do} B \quad ; \quad \overline{v_{nd}^2} = \frac{4kT\gamma g_{do} B}{g_m^2} \quad ; \quad \gamma = 2/3 \text{ for saturation and long channels}$$

$$\overline{i_{ng}^2} = 4kT\gamma g_g B \quad ; \quad g_g = \frac{\omega^2 C_{gs}}{5g_{do}}$$

Correlation coefficient

$$c = \frac{\overline{i_{ng} i_{nd}^*}}{\left[\overline{i_{ng}^2} \cdot \overline{i_{nd}^2} \right]^{1/2}}$$

$$R_n = \frac{v_n^2}{4kTB} = \frac{\gamma g_{do}}{g_m^2}$$

$$Y_c = j\omega C_{gs} + g_m \frac{i_{ngc}}{i_{nd}} = j\omega C_{gs} + \frac{g_m}{g_{do}} c \sqrt{\frac{\delta}{5\gamma}} \omega C_{gs}$$

$$Y_c \cong j\omega C_{gs} \left(1 - \alpha |c| \sqrt{\frac{\delta}{5\gamma}} \right) = jB_c$$

$$G_c \sim 0$$

$$R_n = \frac{\gamma g_{do}}{g_m^2} = \frac{\gamma}{\alpha} \frac{1}{g_m}$$

$$G_u = \frac{\delta \omega^2 C_{gs}^2 (1 - |c|^2)}{5g_{go}} ; \quad \omega_T \cong \frac{g_m}{c_{gs}}$$

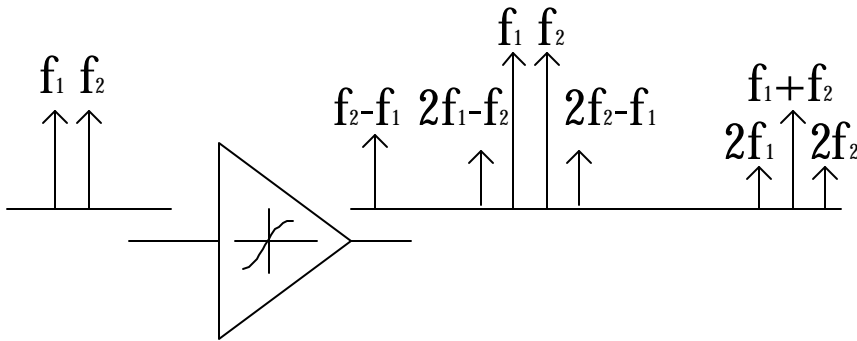
$$B_{opt} = -B_c$$

$$Y_{opt} = G_{opt} + jB_{opt} = G_{opt} - jB_c$$

$$G_{opt} = \sqrt{\frac{G_u}{R_n} + G_c^2} = \alpha \omega C_{gs} \sqrt{\frac{\delta}{5\gamma} (1 - |c|^2)}$$

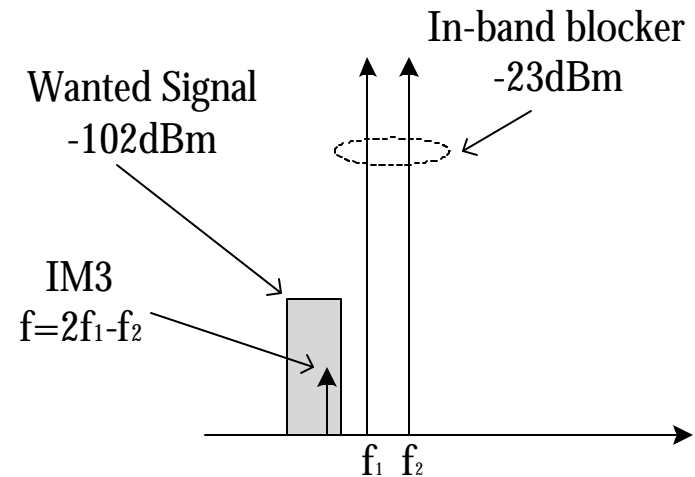
$$F_{min} = 1 + 2R_n [G_{opt} + G_c] \cong 1 + \frac{2\omega}{\sqrt{5\omega_T}} \sqrt{\gamma \delta (1 - |c|^2)}$$

LNA Metrics: Non-linearity model



Output spectrum with two tone input

- Usually distortion term: $2f_1 - f_2$, $2f_2 - f_1$ fall in band. This is characterized by 3rd order non-linearity.
- Large in-band blocker can desensitize the circuit. It is measured by 1-dB compression point.



LNA Metrics: Linearity measurement

□ 1dB compression:

Measure gain compression for large input signal

□ IIP3/IIP2:

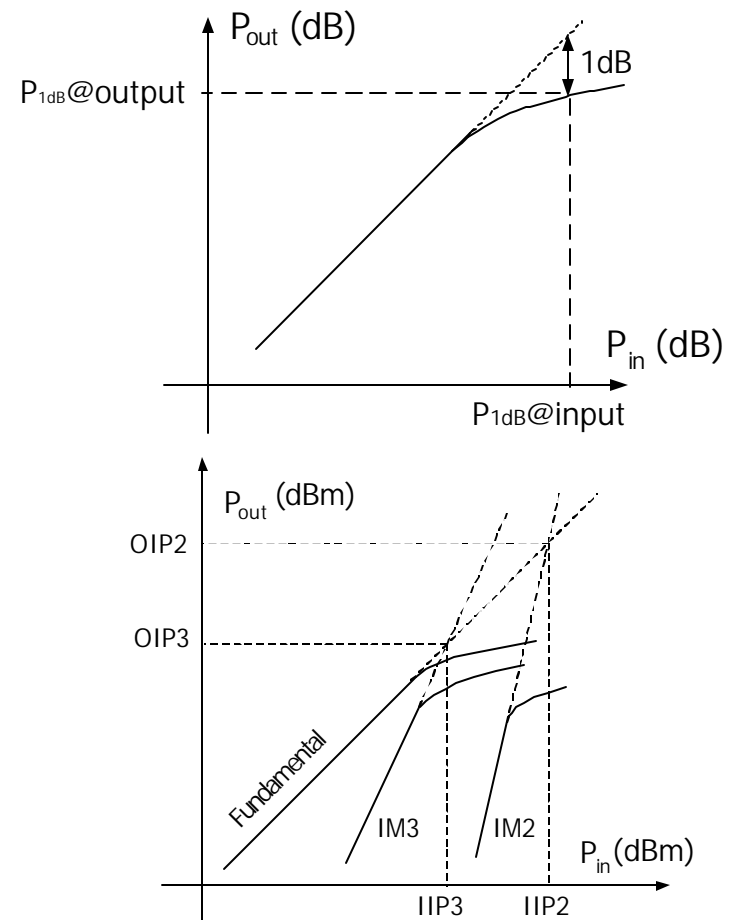
Measure inter-modulation behavior

□ Relationship between IIP3 and P1dB

For one tone test: $IIP3 - P1dB = 10dB$

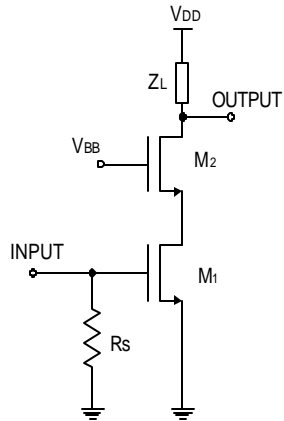
For two tone test: $IIP3 - P1dB = 15dB$

$IIP3 \sim -10dBm \sim 8dBm$



CMOS LNA Topologies

Resistive Termination

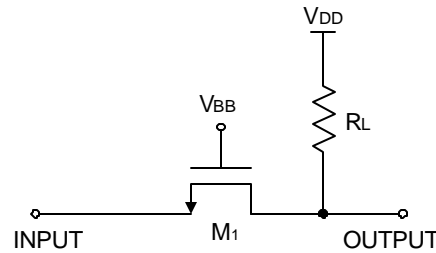


$$Z_{in} = R_s$$

$$F \geq 2 + \frac{4g}{a} \frac{1}{g_{m1}R_s}$$

NF: > 6dB

Common Gate

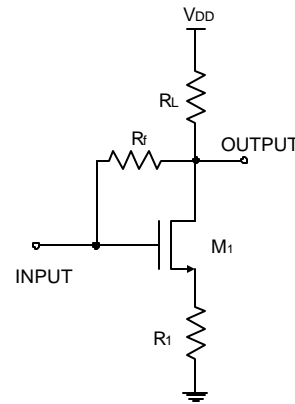


$$Z_{in} = \frac{1}{g_{m1}}$$

$$F \geq 1 + \frac{g}{a}$$

4.8dB

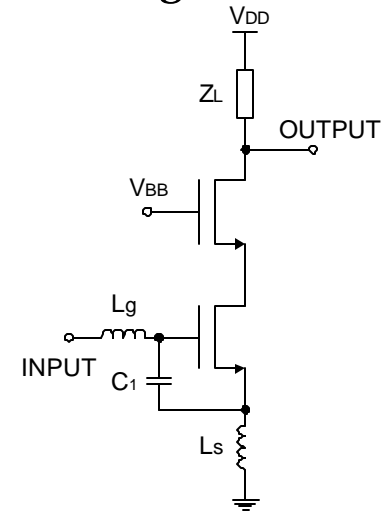
Shunt-series Feedback



$$Z_{in} \approx \frac{R_f}{1 + \frac{R_L}{R_1}}$$

Moderate

Source Degeneration



$$Z_{in} = j\omega(L_g + L_s) + \frac{1}{j\omega C_{gs}} + \frac{g_m}{C_{gs}} L_s$$

< 2dB

LNA Topologies (cont'd)

- ❑ Narrowband LNA: inductive degenerated
- ❑ Broadband LNA: common-gate and series-shunt feedback
- ❑ Bipolar LNAs also have corresponding configurations

Focusing on inductive degenerated LNA

- ❑ Input match
- ❑ Noise match
- ❑ Linearity

A Popular Narrow Band LNA: Inductive Source Degenerated LNA

Source Degenerated LNA

Input impedance

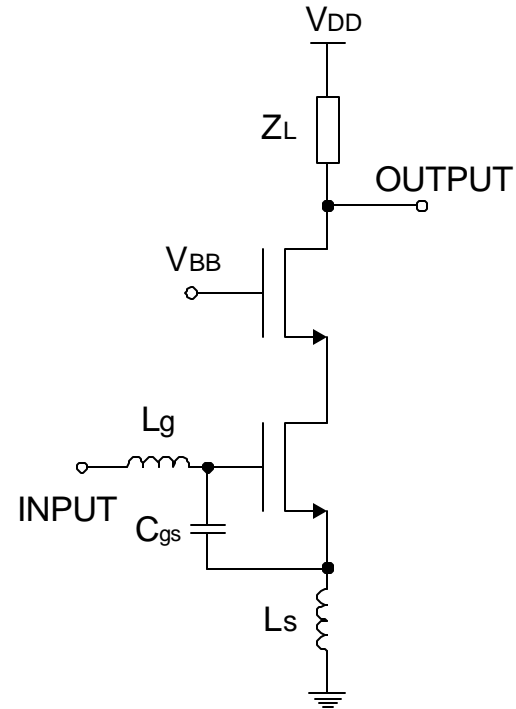
$$Z_{in} = j\omega(L_g + L_s) + \frac{1}{j\omega C_{gs}} + \frac{g_m}{C_{gs}} L_s$$

$$\omega_o = \frac{1}{\sqrt{(L_g + L_s)C_{gs}}} \quad \omega_T = \frac{g_m}{C_{gs}}$$

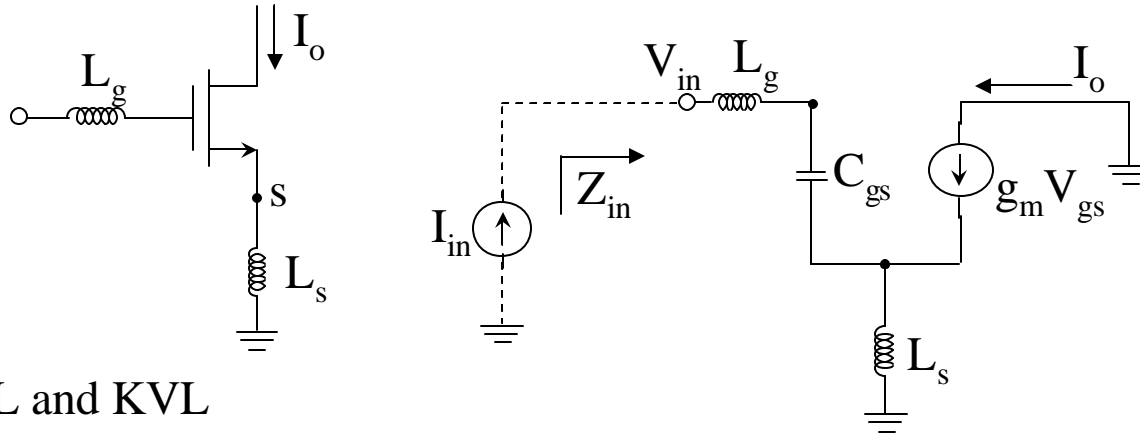
$$Z_o = \omega_T L_s$$

Z_o : 50Ohm, 75Ohm

ω_o : 900MHz, 1.9GHz, 2.4GHz, 5GHz



SOURCE DEGENERATED LNA ANALYSIS



Writing KCL and KVL

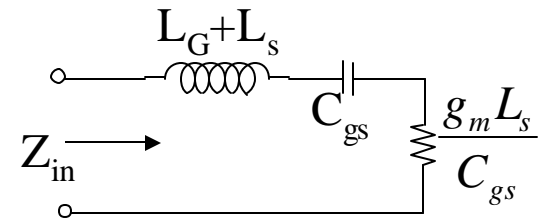
$$I_o = g_m V_{gs} = I_{in} \times \frac{1}{sC_{gs}} g_m = \frac{g_m}{sC_{gs}} I_{in} \quad (1)$$

$$V_{in} = \left[s(L_g + L_s) + \frac{1}{sC_{gs}} \right] I_{in} + I_o sL_s \quad (2)$$

Solving (1) and (2)

$$Z_{in} = \frac{V_{in}}{I_{in}} = s(L_G + L_S) + \frac{1}{sC_{gs}} + \frac{g_m L_S}{C_{gs}}$$

$$Z_{in}(j\omega) = j \left[(L_G + L_S)\omega - \frac{1}{\omega C_{gs}} \right] + \frac{g_m L_S}{C_{gs}}$$



Matching occurs when $Z(j\omega_o)=R_s$, R_s is the resistor associated in the input voltage source. That is

$$(L_G + L_S)\omega_o = \frac{1}{\omega_o C_{gs}} \quad ; \quad \omega_o^2 = \frac{1}{(L_G + L_S)C_{gs}}$$

and

$$R_s = \frac{g_m L_S}{C_{gs}}$$

which implies that :

$$L_G = \frac{1}{\omega_o^2 C_{gs}} - L_S$$

Matching occurs when $Z(j\omega_o)=R_s$, R_s is the resistor associated in the input voltage source. That is

$$(L_G + L_S)\omega_o = \frac{1}{\omega_o C_{gs}} \quad ; \quad \omega_o^2 = \frac{1}{(L_G + L_S)C_{gs}}$$

and

$$R_s = \frac{g_m L_S}{C_{gs}}$$

which implies that :

$$L_G = \frac{1}{\omega_o^2 C_{gs}} - L_S$$

$$Z_{in}(j\omega_o) = \frac{g_m L_s}{C_{gs}} = R_o$$

$$V_{gs} = I_{in} \times \frac{1}{sC_{gs}}$$

$$V_{in}(j\omega_o) = Z_{in}(j\omega_o) \cdot I_{in}(j\omega_o) = R_o I_{in}(j\omega_o)$$

Thus

$$\frac{V_{gs}(s)}{V_{in}(s)} = \frac{1}{j\omega_o R_o C_{gs}} = \frac{-j}{\omega_o R_o C_{gs}}$$

$$G_m(s) = \frac{I_o(s)}{V_{in}(s)} = \frac{1}{s^2 + s \frac{L_s g_m}{(L_g + L_s) C_{gs}} + \frac{1}{(L_g + L_s) C_{gs}}}$$

$$\frac{\omega_o}{Q} = \frac{g_m L_s}{(L_g + L_s) C_{gs}} = \frac{R_o}{(L_g + L_s) C_{gs}} \quad ; \quad Q = \frac{1}{R_o} \sqrt{\frac{L_g + L_s}{C_{gs}}} = \frac{1}{\omega_o R_o C_{gs}}$$

Recall that

$$I_o = -g_m V_{gs} = G_m V_{in} \quad , \quad g_m = G_m \frac{V_{in}}{V_{gs}} = +G_m = -jQg_m \quad , \quad |G_m|^2 = Q^2 g_m^2$$

The input voltage referred noise

$$\overline{v_i^2} = \frac{\overline{i_d^2}}{|G_m|^2} = \frac{\frac{2}{3}4kTg_m}{g_m^2 Q^2}$$

Thus

$$NF = 1 + \frac{\frac{8}{3}kTg_m}{g_m^2 Q^2 (4kTR_s)} = 1 + \frac{2}{3} \frac{1}{g_m Q^2 R_s}$$

$$NF = 1 + \frac{2}{3} \frac{L_s}{(L_g + L_s)} \cong 1 + \frac{2}{3} \frac{L_s}{L_g}$$

Source Degenerated LNA (cont'd)

Input impedance-non-idealities

$$Z_{in} = j\omega(L_g + L_s) + \frac{1}{j\omega C_{gs}} + \frac{1}{j\omega \frac{1}{\omega_T R_{Ls}}} + \omega_T L_s + R_{Lg} + R_g + R_{Ls} + R_{g,NQS}$$

$$\omega_o = \frac{1}{\sqrt{(L_g + L_s) \left(C_{gs} \parallel \frac{1}{\omega_T R_{Ls}} \right)}} \quad \omega_T = \frac{g_m}{C_{gs}}$$

$$Z_{in} = \omega_T L_s + R_{Lg} + R_g + R_{Ls} + R_{g,NQS}$$

Inductance loss: R_{Lg} : offset Z_{in}

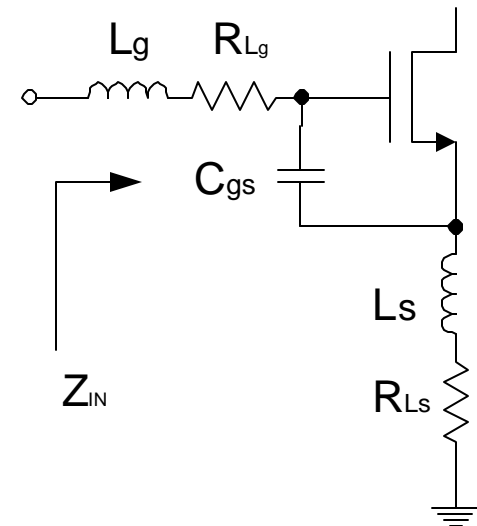
R_{Ls} : offset Z_{in} and ω_o

Gate resistance R_g : offset Z_{in}

NQS gate resistance: R_{nqs} : offset Z_{in}

$$R_g = \frac{R_{poly,sh} W}{12n^2 L}$$

$$R_{g,NQS} = \frac{1}{5g_m}$$



Source Degenerated LNA (cont'd)

Noise factor

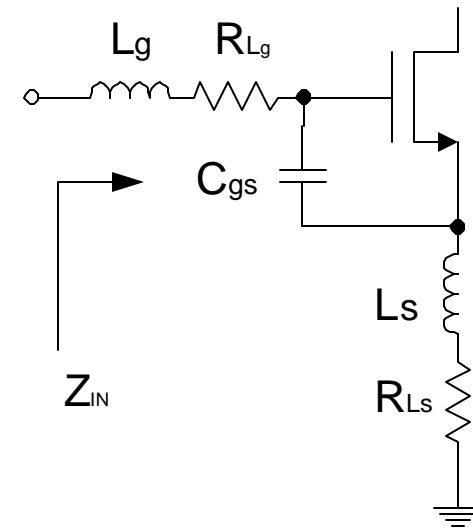
$$F = 1 + \frac{R_L}{R_s} + \frac{R_g}{R_s} + \frac{g}{a} \frac{c}{Q_L} \left(\frac{w_o}{w_T} \right)$$

$$Q_L = \frac{w_o (L_s + L_g)}{R_s} = \frac{1}{w_o R_s C_{gs}}$$

$$c = 1 + 2|c|Q_L \sqrt{\frac{da^2}{5g}} + \frac{da^2}{5g} (1 + Q_L^2)$$

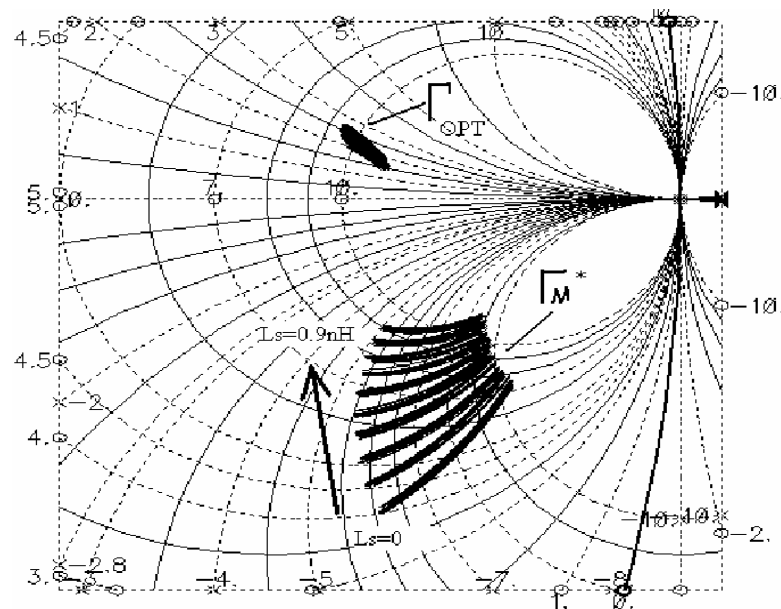
There is an optimal Q_L to minimize F

Is this F the minimum achievable one?



Source Degenerated LNA (cont'd)

Achieve minimum noise figure: trading input match



$$F = F_{\min} + \frac{R_n}{G_s} |Y_s - Y_{opt}|^2$$

Inductive Source degeneration:

The degeneration inductance modifies the input reflection coefficient without affecting the optimal input reflection coefficient for minimum noise figure.

Source Degenerated LNA (cont'd)

Linearity

Different width of transistor

$$V_{IIP3, strong, MOS}^2 = \frac{4}{3} \frac{V_{eff}}{q} (2 + qV_{eff})(1 + qV_{eff}) > \frac{8}{3} \frac{V_{eff}}{q}$$

$$V_{eff} = V_{GS} - V_{th} \quad q = \frac{1}{E_{sat} L}$$

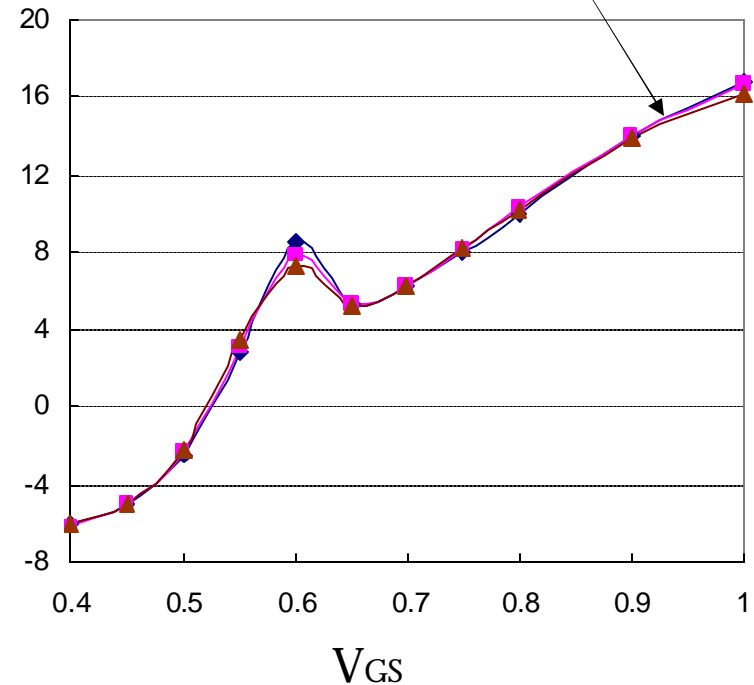
□ IIP3 independent of W

$$V_{IIP3, LNA}^2 (V^2) = \frac{16}{3} \frac{P_D^2}{P_o^2 q^2} (2 + r) \left(1 + \frac{1}{r}\right)^3$$

$$r = qV_{eff} \quad P_o = \frac{3}{2} \frac{v_{sat} E_{sat}}{w_o R_s} V_{DD}$$

$E_{sat} \sim 1V/\mu m$ $L \sim 0.35\mu m - 0.18\mu m$

IIP3 (dBm)



MOS transistor's IIP3 v.s. gate drive voltage

Source Degenerated LNA

(cont'd)

Differential v.s. Single-ended

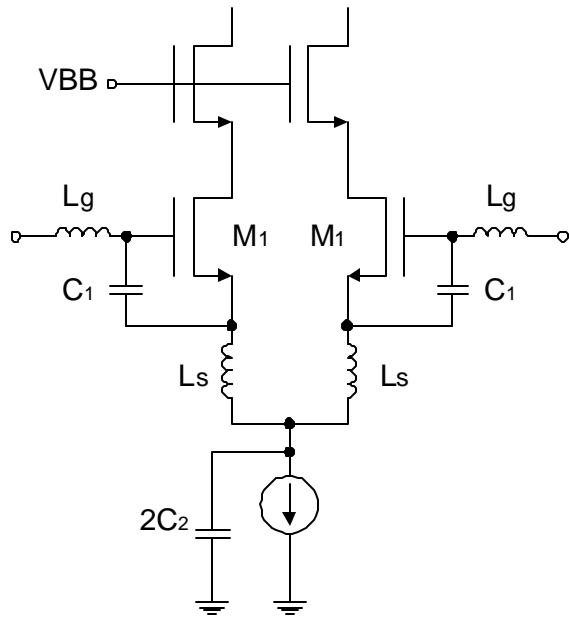
Differential

- ✓ reject common mode noise and interferer
- ✗ double area and current
- ✓ shield the bond wire
- ✗ need balun at input
- ✗ common-mode stability
- ✗ linearity limited by bias current

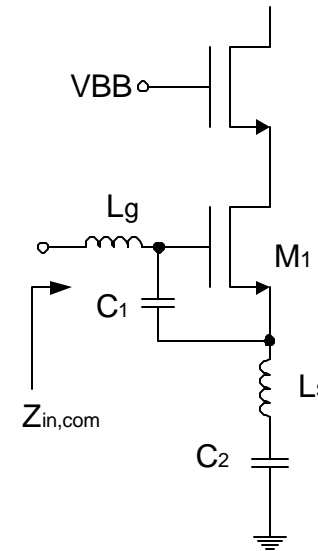
Single-ended

- ✓ compact layout size
- ✓ less power for same NF and linearity
- ✗ susceptible to bond wire and PCB trace
- drive single-balance mixer
- output balun drive double-balance mixer

Differential LNA Common-mode Stability Issue



Typical differential LNA



Common-mode half circuit

$$Z_{in,com} = j\omega(L_g + L_s) + \frac{C_1 + C_2}{j\omega C_1 C_2} + \frac{g_m}{C_1} L_s - \frac{g_m}{\omega^2 C_1 C_2}$$

Differential LNA Common-mode Stability Issue (cont'd)

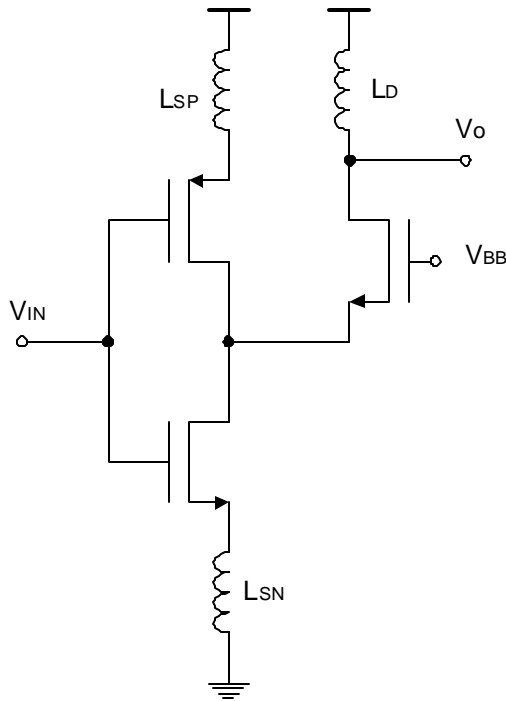
$$Z_{in,com} = j\omega(L_g + L_s) + \frac{C_1 + C_2}{j\omega C_1 C_2} + \frac{g_m}{C_1} L_s - \frac{g_m}{\omega^2 C_1 C_2}$$

Real part:

$$R_{in,com} = \frac{g_m}{C_1} \left(L_s - \frac{1}{\omega^2 C_2} \right)$$

- ❑ For passive termination, the real part of the source impedance will always be positive. IF $R_{in,com}$ happens to be negative and cancel the real part of source impedance, oscillation **MAY** occur.
- ❑ When design differential LNA, not only pay attention to differential operation, but also check common-mode stability!

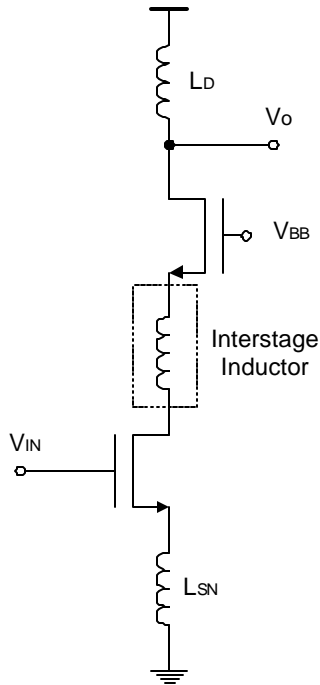
Variant of Inductive Degenerated LNA



Single-ended version of current-reuse LNA (bias not shown)

- nMOS-pMOS shunt input
- Current reuse to save power
- Larger area due to two degeneration inductor if implemented on chip
- NF: 2dB, Power gain: 17.5dB, IIP3: -6dBm, I_d : 8mA from 2.7V power supply

Variant of Inductive Degenerated LNA (cont'd)



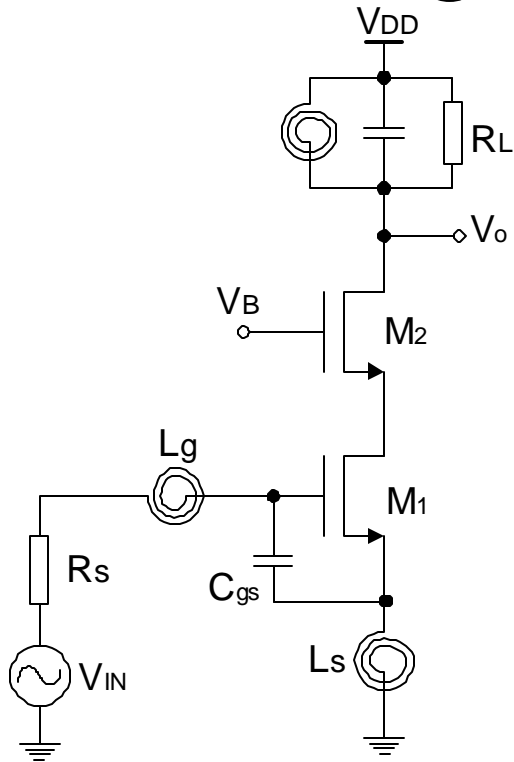
❑ Inter-stage inductor with parasitic capacitance form impedance match network between input stage and cascoded stage boost gain lower noise figure.

❑ Input match condition will be affected

Inter-stage Inductor gain boost

Design Procedure for Inductive Source Degenerated LNA

Targeting Structure



Inductively degenerated
CMOS LNA

Noise factor equations:

$$F = 1 + \mathbf{k}_{nf} \left(\frac{\mathbf{w}_0}{\mathbf{w}_T} \right)$$

$$\mathbf{k}_{nf} = \frac{\mathbf{g}}{\mathbf{a}} \frac{1}{2Q} \left[1 - 2|c| \mathbf{c}_d + 4(Q^2 + 1) \mathbf{c}_d^2 \right]$$

$$Q = \frac{1}{2R_s \mathbf{w}_0 C_{gs}} \quad \mathbf{c}_d = \mathbf{a} \sqrt{\frac{\mathbf{d}}{5\mathbf{g}}}$$

Linearity:

$$IIP3 \propto V_{gs} - V_{th}$$

Voltage Gain:

$$A_V = j \left(\frac{\mathbf{w}_T}{\mathbf{w}_0} \right) \frac{R_L}{R_s}$$

Targeted Specifications

Frequency	2.4 GHz ISM Band
Noise Figure	1.6 dB
IIP3	-8 dBm
Voltage gain	20 dB
Power	< 10mA from 1.8V

Step 1: Know your process

□ A 0.18 μ m CMOS Process:

Process related ← $\left\{ \begin{array}{l} - t_{ox} = 4.1e-9 \mu\text{m} \\ \epsilon = 3.9 \cdot (8.85e-12) \text{F/m} \\ \mu = 3.274e-2 \text{m}^2/\text{V}\cdot\text{s} \\ - V_{th} = 0.52 \text{V} \end{array} \right.$

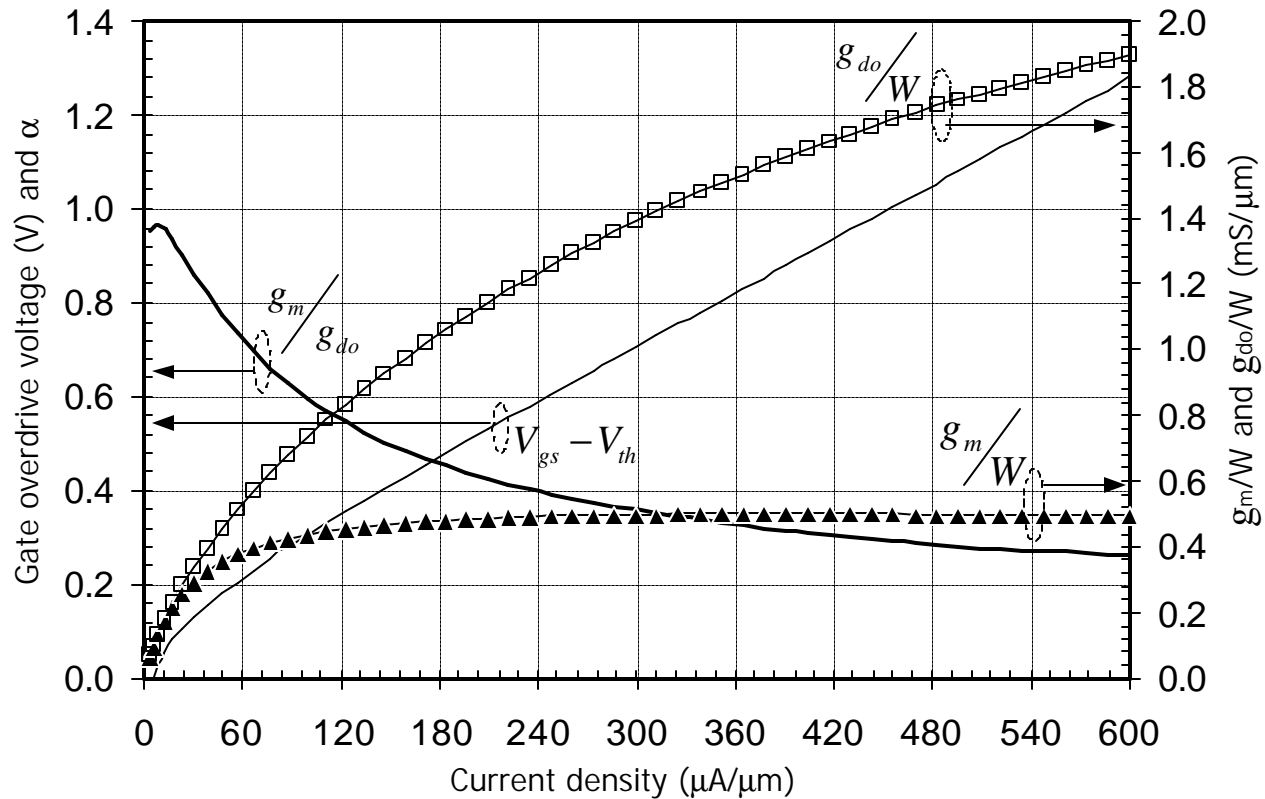
Noise related ← $\left\{ \begin{array}{l} \alpha = g_m/g_{do} \\ \delta/\gamma \sim 2 \\ \gamma \sim 3 \end{array} \right.$

– $c = -j0.55$

Important design guide plots obtained from simulation or measurements

Step 2: Obtain design guide plots

g_m , g_{do} , α , $V_{gs} - V_{th}$ vs. current density plot



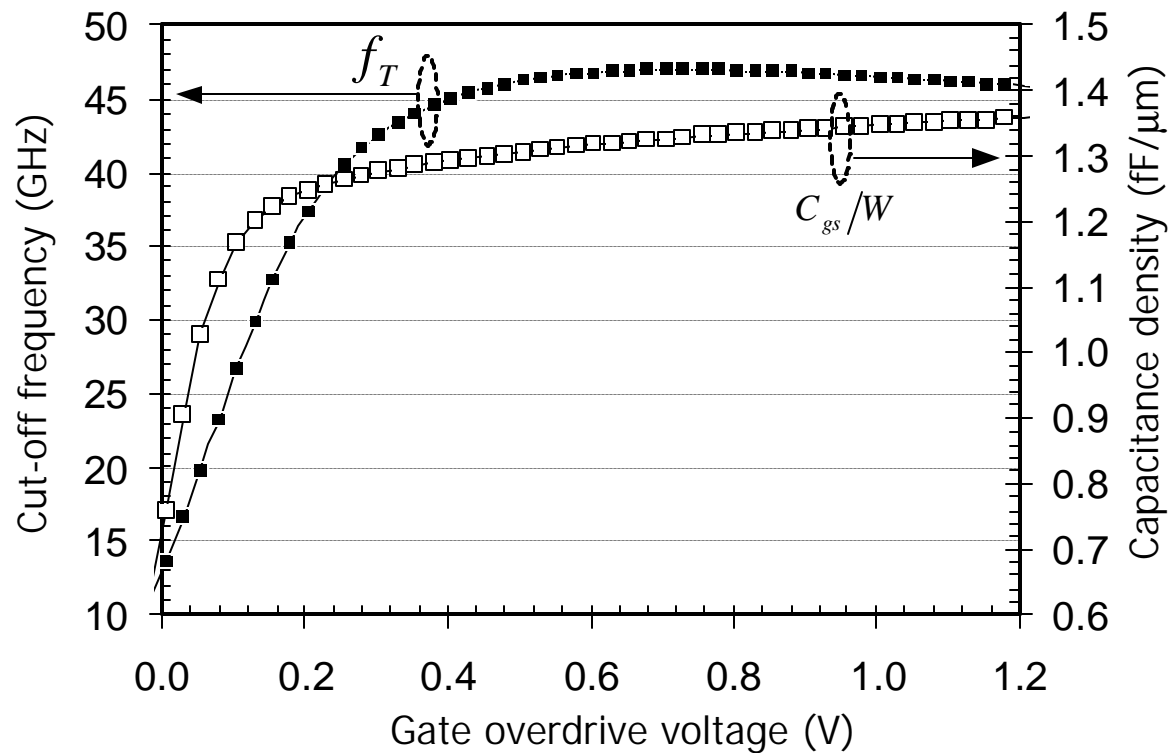
Step 2: Obtain design guide plots (cont'd)

Insights:

- g_{do} increases all the way with current density I_{den}
 - g_m saturates when I_{den} larger than $120\mu A/\mu m$
 - Velocity saturation, mobility degradation ---- short channel effects
 - Low g_m /current efficiency
 - High linearity
- α deviates from long channel value (1) with large I_{den}

Step 2: Obtain design guide plots (cont'd)

f_T and C_{gs} vs. gate overdrive voltage



Step 2: Obtain design guide plots (cont'd)

Insights:

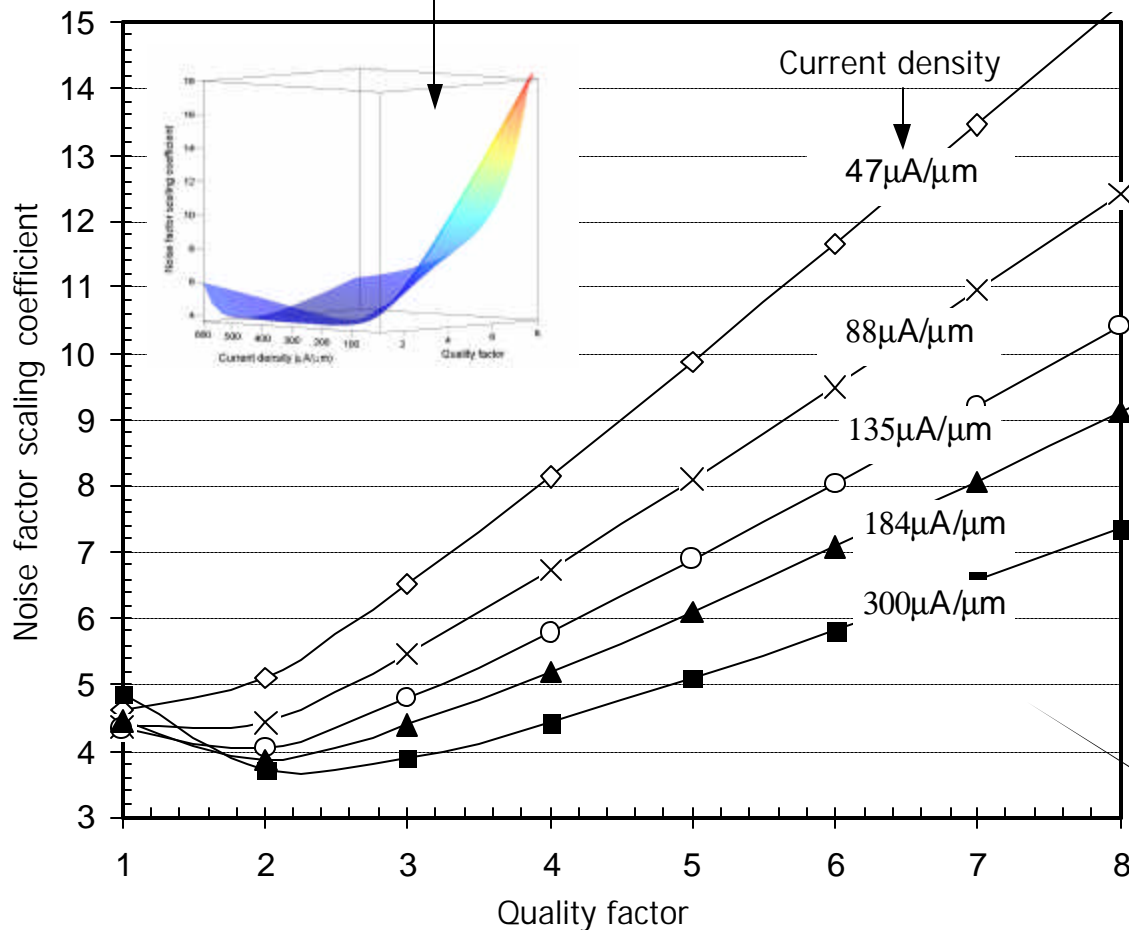
- f_T increases with V_{od} when V_{od} is small and saturates after $V_{od} > 0.3V$ --- short channel effects
- C_{gs}/W increases slowly after $V_{od} > 0.2V$
- f_T begins to degrade when $V_{od} > 0.8V$
 - g_m saturates
 - C_{gs} increases

Step 2: Obtain design guide plots

(cont'd)

K_{nf} vs input Q and current density

3-D plot for visual inspection



$$F = 1 + k_{nf} \left(\frac{w_0}{w_T} \right)$$

$$Q = \frac{1}{2R_s w_0 C_{gs}}$$

2-D plots for design reference

Step 2: Obtain design guide plots (cont'd)

Insights:

Design trade-offs

$I_{den}?$ - $F?$

$Q?$ - $F?$

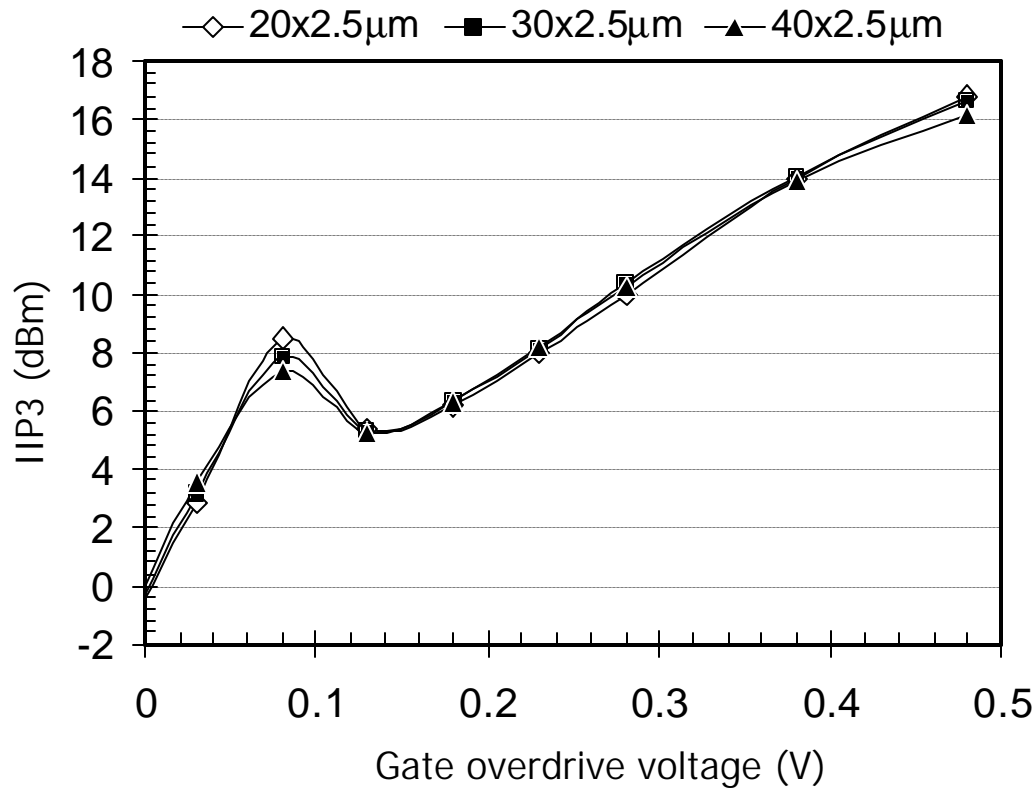
For large I_{den} ($300 \mu\text{A}/\mu\text{m}$) there is an optimal value of Q --- maybe too large for a practical design

For fixed I_{den} , increasing Q will reduce the size of transistor thus reduce total power ---- noise figure will become larger

Step 2: Obtain design guide plots

(cont'd)

Linearity plots :IIP3 vs. gate overdrive and transistor size



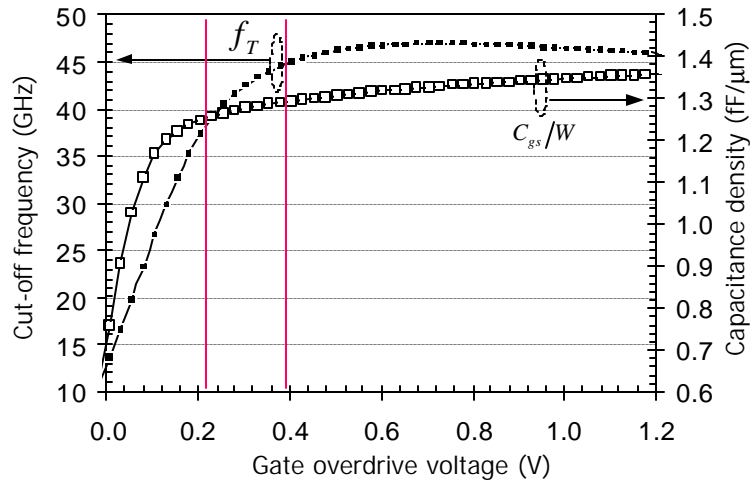
Step 2: Obtain design guide plots (cont'd)

Insights:

- MOS transistor IIP3 only, when embedded into actual circuit:
 - Input Q will degrade IIP3
 - Non-linear memory effect will degrade IIP3
 - Output non-linearity will degrade IIP3
- IIP3 is a very weak function of device size
- Generally, large overdrive means large IIP3
 - But the relationship between IIP3 and gate overdrive is not monotonic
 - There is a local maxima around 0.1V overdrive

Step 3: Estimate f_T and calculate

K_{nf}



$$f_o = 2.4 \text{ GHz} \quad F = 1.45$$

$$k_{nf} = (F - 1) \frac{f_o}{f_T} = 7.5$$

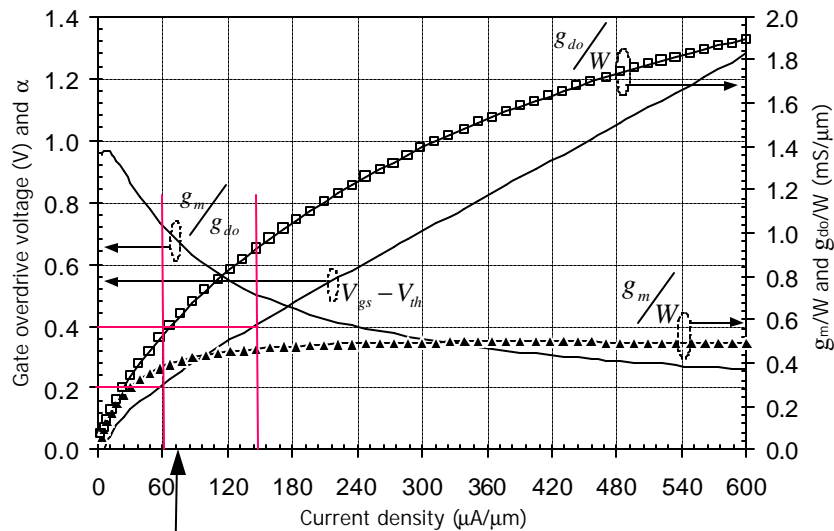
□ Small current budget ($< 10\text{mA}$)
does not allow large gate over drive :

□ $0.2 \text{ V} \sim 0.4 \text{ V}$

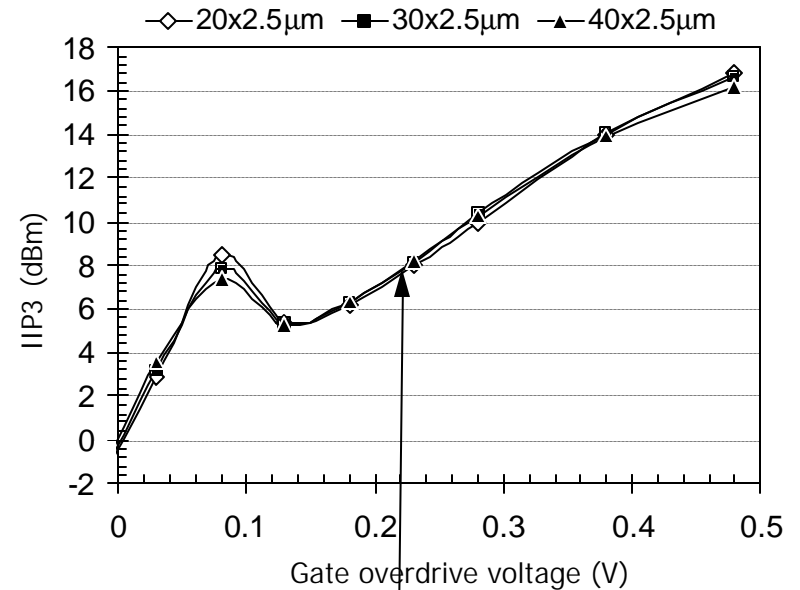
□ $f_T \sim 40 \text{ GHz}$

$$C_{gs}/W = 1.3 \text{ fF} / \mu\text{m}$$

Step 4: Determine I_{den} , Q and Calculate Device Size



Select $I_{den} = 70 \mu\text{A}/\mu\text{m}$



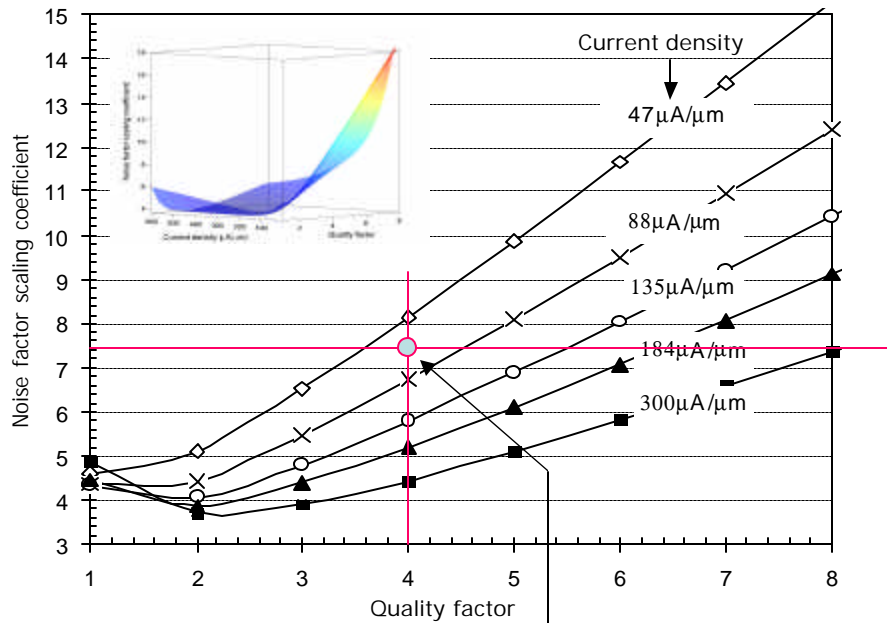
If $Q = 4$, IIP3 will have enough margin:

Estimated IIP3:

$IIP3(\text{read from curve}) - 20\log(Q) \sim -4\text{dBm}$

Specs require: -8 dBm

Step 4: Determine I_{den} , Q and Calculate Device Size (cont'd)



$Q=4$ and $I_{den} = 70\mu\text{A}/\mu\text{m}$ meet the noise factor requirement

Now we can do calculations:

$$C_{gs} = \frac{1}{2QR_s w_o} \sim 166 \text{ fF}$$

$$W = \frac{166 \text{ fF}}{1.3 \text{ fF} / \text{mm}} = 128 \text{ mm}$$

$$I_{DS} = 128 \text{ mm} \times 70 (\text{mA} / \text{mm}) = 8.9 \text{ mA}$$

Step 5: Calculate L_g , L_s and Required Load

- Verify cut-off frequency
 - g_m is about 50mA/V for the determined current density and device size
 - $f_T = g_m / (C_{gs} * 2\pi) = 48 \text{ GHz}$ --- Verified !
-

$$L_s = \frac{R_s}{\omega_T} \approx 0.2 \text{ nH}$$

$$L_g = \frac{1}{\omega_o^2 C_{gs}} - L_s \approx 26 \text{ nH}$$

$$A_V = j \left(\frac{\omega_T}{\omega_o} \right) \frac{R_L}{R_s}$$



$$R_L = \frac{\omega_o}{\omega_T} |A_V| R_s \approx 30 \Omega$$

Step 6: Simulation Verification

Usually simulation-hand calculation iterations are necessary to obtain satisfactory design

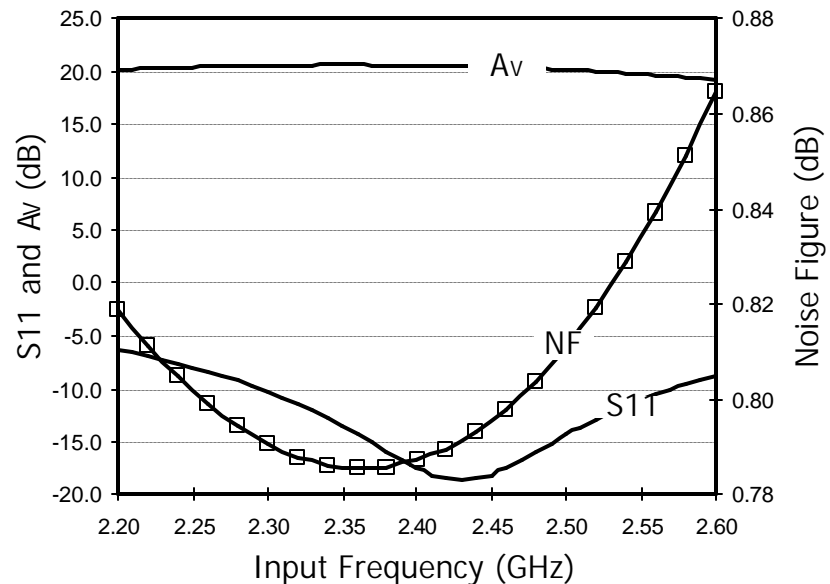
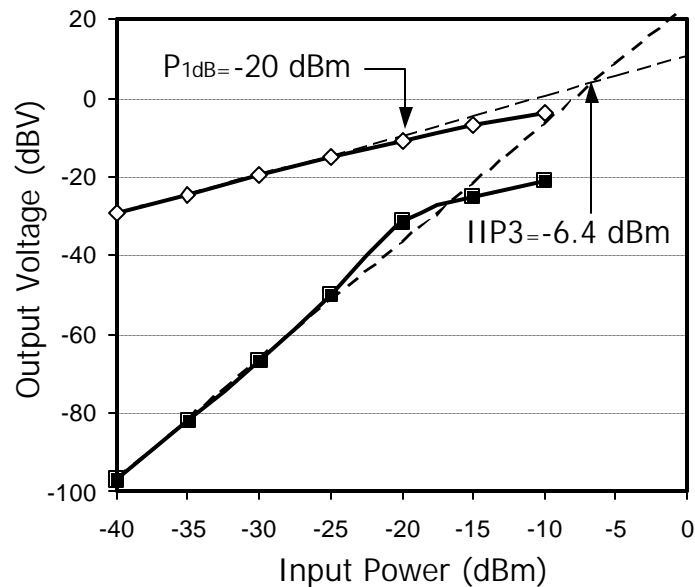
Parameters	Calculation	Simulation
W	128um	127.5um
I _{ds}	8.9mA	8mA
g _m	50mA/V	50.7mA/V
C _{gs}	166fF	151fF
L _s	0.2nH	0.2nH
L _g	26nH	16nH
R _L	30 Ohm	40 Ohm

Deviate from hand-calculation most

Possible reason:
C_{gd} is not considered for hand calculation

Step 6: Simulation Verification (cont'd)

Simulation plots for IIP3, A_v , NF and S11



Step 6: Simulation Verification (cont'd)

Comparison between targeted specs and simulation results

Parameter	Target	Simulated
Noise Figure	1.6 dB	0.8 dB
Current	< 10mA	8 mA
Voltage gain	20 dB	21 dB
IIP3	-8 dBm	-6.4 dBm
P1dB	---	-20dbm
S11	---	-17 dB
Power Supply	1.8V	1.8V

Summary for LNA Design Procedure

- ❑ Design mixed with simplified equations and simulation plots normalized to unity device size help to gain insights and consider all the important design specification at the same time.
- ❑ Several iterations is generally required from hand calculation to simulation to arrive at satisfactory or optimal design.
- ❑ Secondary effects such as gate poly resistance can be considered during simulation and can also be considered by add more margin in the design specifications.