

ELEN 458 Lab 1

OP AMP Characterization

Objective

A student must become familiar with the practical limitations of op amp and some measuring techniques because some of the measuring techniques that are used in simulations are not possible in laboratory. This will incorporate some basic op amp configurations.

Component List

- 741 op amp
- Resistors – 5.1k, 27k, 100k, 10k, 1k, ?
- Capacitors - ?

Prelab

Perform simulations using PSPICE and the LM741 macromodel* for the following lab procedure

- Output Voltage Swing
- Settling Time
- Slew Rate (Apply a 10 Vpp square wave at 10kHz)
- Gain-Bandwidth Properties
- Phase Margin
- Offset Voltage
- Open Loop Gain

Lab Procedure

The power supplies for the entire lab will be $\pm 15V$ and graph all data sets. Answers all questions and add any other prudent material in the lab report.

Note: the macromodel can be found on the last page of this lab.

Output Voltage Swing

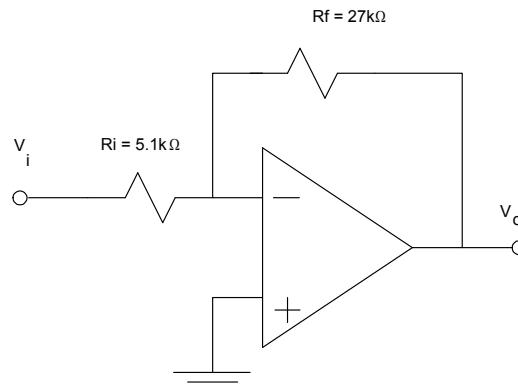


Figure 1

Construct figure 1 and apply input voltage from $-4V$ to $4V$ in increments of $0.5V$ and plot results of V_o vs V_i . Now, apply a $2V_{pp}$ sinusoidal at $1kHz$ and slowly increase the amplitude until distortion occurs. Try measuring the distortion with the THD machine and in simulation find the amplitudes where there is one, five and ten percent THD. What is the function of the circuit, and why is the graph clipping at the edges? What is the maximum voltage swing?

Settling Time & Slew Rate

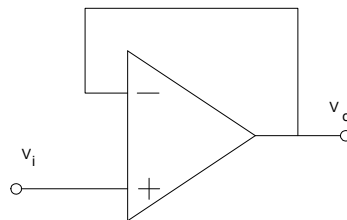


Figure 2

Construct figure 2 and apply square wave with an amplitude of $0.2 V_{pp}$ at $100kHz$ to the input. Observe and adjust V_o on the oscilloscope until damped oscillations are obtained. Determine the time it takes the output step to settle to within one percent of the final value. What is the function of the circuit, and what is causing the damped oscillations in the output of the waveform?

Now apply a square wave with an amplitude of $10 V_{pp}$ at $100Hz$ and slowly increase the frequency until the output waveform begins to distort. Using the cursors of the oscilloscope calculate the slew rate in $V/\mu sec$. What is causing the op amp to slew?

Offset Voltage

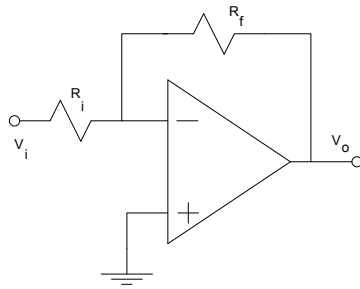


Figure 4

Using the inverting configuration in figure 4, let R_f be $100\text{k}\Omega$ and R_i be $10\text{k}\Omega$. Now ground the input and measure the output voltage. This is the DC offset voltage. Now add a $25\text{k}\Omega$ potentiometer to the null pins of the op amp and adjust the resistance till the DC offset has been eliminated. What causes the DC offset and how does the potentiometer compensate for that? How can we measure the DC offset for the non-inverting amplifier configuration and an alternate way to reduce DC offset for the configuration?

Gain-Bandwidth Properties & Phase Margin

Change R_f to $5.1\text{k}\Omega$ and R_i to $1\text{k}\Omega$ and remove the potentiometer. Now, apply a 0.2Vpp sinusoidal signal to the input and vary the frequency from 100Hz to 1MHz while gathering data points of the V_o and determining the phase. Be sure to determine unity gain frequency and 3dB frequency. Plot the magnitude and phase vs frequency and indicate the important features. Repeat this process for R_f equal to $271\text{k}\Omega$. What is the relation of gain to the bandwidth in an op amp? What information can phase give about a op amp, filter, or any other system?

Open Loop Gain

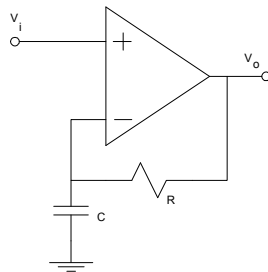


Figure 5

Figure 5 will be used to determine the open loop gain of the op amp. Apply a small sinusoidal signal at the input and measure the output with different frequencies ranging from 100Hz to 10MHz (make RC the dominant pole). If possible, measure the phase. Why is the open loop gain finite rather than infinite, as it would be for an ideal op amp?

LM741

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* amps-apps@galaxy.nsc.com

*////////////////////////////////////

*LM741 OPERATIONAL AMPLIFIER MACRO-MODEL

*////////////////////////////////////

*
* connections: non-inverting input
* | inverting input
* | | positive power supply
* | | | negative power supply
* | | | | output
* | | | | |
* | | | | |
* | | | | |

.SUBCKT LM741/NS 1 2 99 50 28

*
*Features:
*Improved performance over industry standards
*Plug-in replacement for LM709,LM201,MC1439,748
*Input and output overload protection
*

*****INPUT STAGE*****

*
IOS 2 1 20N
*^Input offset current
R1 1 3 250K
R2 3 2 250K
I1 4 50 100U
R3 5 99 517
R4 6 99 517
Q1 5 2 4 QX
Q2 6 7 4 QX
*Fp2=2.55 MHz
C4 5 6 60.3614P
*

*****COMMON MODE EFFECT*****

*
I2 99 50 1.6MA
*^Quiescent supply current

```

EOS 7 1 POLY(1) 16 49 1E-3 1
*Input offset voltage.^
R8 99 49 40K
R9 49 50 40K
*
*****OUTPUT VOLTAGE LIMITING*****
V2 99 8 1.63
D1 9 8 DX
D2 10 9 DX
V3 10 50 1.63
*
*****SECOND STAGE*****
*
EH 99 98 99 49 1
G1 98 9 5 6 2.1E-3
*Fp1=5 Hz
R5 98 9 95.493MEG
C3 98 9 333.33P
*
*****POLE STAGE*****
*
*Fp=30 MHz
G3 98 15 9 49 1E-6
R12 98 15 1MEG
C5 98 15 5.3052E-15
*
*****COMMON-MODE ZERO STAGE*****
*
*Fpcm=300 Hz
G4 98 16 3 49 3.1623E-8
L2 98 17 530.5M
R13 17 16 1K
*
*****OUTPUT STAGE*****
*
F6 50 99 POLY(1) V6 450U 1
E1 99 23 99 15 1
R16 24 23 25
D5 26 24 DX
V6 26 22 0.65V
R17 23 25 25
D6 25 27 DX
V7 22 27 0.65V
V5 22 21 0.18V
D4 21 15 DX
V4 20 22 0.18V
D3 15 20 DX
L3 22 28 100P
RL3 22 28 100K
*
*****MODELS USED*****
*
.MODEL DX D(IS=1E-15)
.MODEL QX NPN(BF=625)
*
.ENDS

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LM13600

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* //////////////////////////////////

* LM13600 Dual Operational Transconductance Amplifier

* //////////////////////////////////

*
* Amplifier Bias Input
* | Diode Bias
* || Positive Input
* ||| Negative Input
* |||| Output
* ||||| Negative power supply
* ||||| Buffer Input
* ||||| Buffer Output
* ||||| Positive power supply
* |||||

.SUBCKT LM13600/NS 1 2 3 4 5 6 7 8 11

*
* Features:
* gm adjustable over 6 decades.
* Excellent gm linearity.
* Linearizing diodes.
* Controlled impedance buffers.
* Wide supply range of +/-2V to +/-22V.
*

* Note: This model is single-pole in nature and over-estimates
* AC bandwidth and phase margin (stability) by over 2X.
* Although refinement may be possible in the future, please
* use benchtesting to finalize AC circuit design.
*

* Note: Model is for single device only and simulated
* supply current is 1/2 of total device current.
*

*
C1 6 4 4.8P
C2 3 6 4.8P
* Output capacitor

```

C3 5 6 6.26P
D1 2 4 DX
D2 2 3 DX
D3 11 21 DX
D4 21 22 DX
D5 1 26 DX
D6 26 27 DX
D7 5 29 DX
D8 28 5 DX
D10 31 25 DX
* Clamp for -CMR
D11 28 25 DX
* Ios source
F1 4 3 POLY(1) V6 1E-10 5.129E-2 -1.189E4 1.123E9
F2 11 5 V2 1.022
F3 25 6 V3 1.0
F4 5 6 V1 1.022
F5 30 6 V3 1.0
* Output impedance
F6 5 0 POLY(2) V3 V7 0 0 0 0 1
G1 0 33 5 0.55E-3
I1 11 6 300U
Q1 24 32 31 QX1
Q2 23 3 31 QX2
Q3 11 7 30 QX1
Q4 11 30 8 QY
V1 22 24 0V
V2 22 23 0V
V3 27 6 0V
V4 11 29 1.4
V5 28 6 1.2
V6 4 32 0V
V7 33 0 0V
.MODEL QX1 NPN (IS=5E-16 BF=200 NE=1.15 ISE=.63E-16 IKF=1E-2)
.MODEL QX2 NPN (IS=5.125E-16 BF=200 NE=1.15 ISE=.63E-16 IKF=1E-2)
.MODEL QY NPN (IS=6E-15 BF=140)
.MODEL DX D (IS=5E-16)
.ENDS
*$

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