

Comment

GB-R impedances: New approach to impedance simulation

M. van de Gevel

Indexing terms: Capacitors, Impedance converters, Inductors, Operational amplifiers

In [1], Serrano and Carlosena prove that the input impedances of the circuits in Fig. 1a and b of [1] are independent of C_A and R_B , as long as $C_A R_B \ll 1/GB$. However, this requirement can be fulfilled by making C_A and R_B equal to zero. In this case, two out of three passive components in Fig. 1a of [1] and four out of five passive components in Fig. 1b of [1] can be eliminated. The opamp on the left hand side of Fig. 1b of [1] also becomes redundant, so that the remaining circuit becomes equivalent to that described in [2] (see Fig. 1). Without redundant components, Fig. 1a is a simpler implementation of the R-active circuit described in Table 2d of [3]. Compared with the circuit in [3], Fig. 1a (with or without C_A and R_B) has the advantage of having no floating nodes in the circuit, which gives it a better chance of working in practice.

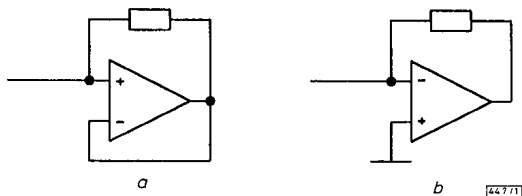


Fig. 1 Simplified capacitance and inductance simulating circuits

a Capacitance simulating
b Inductance simulating

© IEE 1995

24 May 1995

Electronics Letters Online No: 19950956

M. van de Gevel (Delft University of Technology, Faculty of Electrical Engineering, Electronics Research Laboratory, Mekelweg 4, NL-2628 CD Delft, The Netherlands)

References

- SERRANO, L., and CARLOSENA, A.: 'GB-R impedances: New approach to impedance simulation', *Electron. Lett.*, 1995, **31**, (9), pp. 689-690
- ALLEN, J., GUMUSSOY, M., and HOLT, A.G.J.: 'Inductance simulation and filter design using a single-pole amplifier approximation', *Electron. Lett.*, 1978, **14**, (19), pp. 629-631
- ISHIDA, M., FUKUI, Y., and EBITSUNAMI, K.: 'Novel active-R synthesis of a driving point impedance', *Int. J. Electron.*, 1984, **56**, (1), pp. 151-158

Reply

GB-R impedances: New approach to impedance simulation

L. Serrano and A. Carlosena

We thank M. van de Gevel for the comment [1], which gives further insight into the circuits we proposed in [2].

We substantially agree with the comment on [2], in the sense that the two circuits proposed are equivalent to, and much simpler than, our circuits for limited C_A and R_B values. We propose design

conditions such that $R_B C_A \ll 1$, and in the particular case $R_B = 0$ and $C_A = 0$, our circuits in Fig. 1a and b of [2] become the R-active impedances of Fig. 1a and b of [1]. However, retaining R_B and C_A in the designs has several advantages:

(i) From a theoretical perspective, R-active impedances (and in general R-active circuits) can be seen as limiting cases of RC active impedances (circuits). GB-R impedances can be regarded as the transition between both cases.

(ii) The impedance range can be extended. In the example of the capacitor, it can take both positive and negative values, depending on the value of $R_B C_A$, as shown in Fig. 1. For values $< 0.1/GB$, say, the capacitance value is quite independent of the time constant (and controllable with R_1), whereas for larger time constant values R_1 , R_B and C_A can be used to define the capacitance. Similar arguments can be given for simulated inductances, with only positive values.

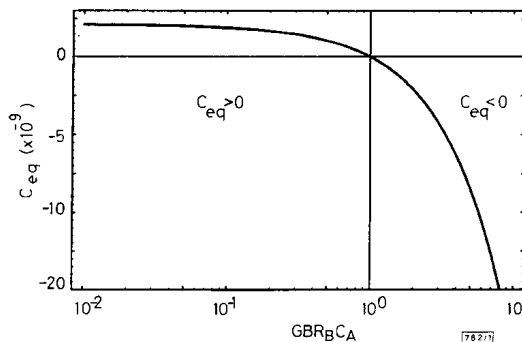


Fig. 1 Capacitor value for R_1 constant and $R_B C_A$ variable

(iii) Even for the intermediate $R_B C_A$ region, with a similar capacitance value to that of the R-active impedances, the use of R_B and C_A provides a slightly better frequency response. In the capacitor example, when $GB R_B C_A = 1/2$, an inherent phase compensation is achieved, for the capacitance value $C_{eq} = 1/(2GB R_1)$.

(iv) In a circuit such as the inductor example of Fig. 1b in [2], which uses two opamps, the first opamp can be used for buffering in the case of ladder (simulated) passive filters [3].

© IEE 1995

20 June 1995

Electronics Letters Online No: 19950957

L. Serrano and A. Carlosena (Universidad Pública de Navarra, Dept. de Automática, Electrónica e Ing. de Sistemas, Pamplona, E-31006 Navarra, Spain)

References

- VAN DE GEVEL, M.: 'Comment: GB-R impedances: New approach to impedance simulation', *Electron. Lett.*, 1995, **31**, (17), pp.
- SERRANO, L., and CARLOSENA, A.: 'GB-R impedances: New approach to impedance simulation', *Electron. Lett.*, 1995, **31**, (9), pp. 689-690
- SCHAUMANN, R., GHAUSI, M.S., and LAKER, K.R.: 'Design of analog filter: Passive, active RC and switched capacitor' (Prentice-Hall, 1990)

Macromodel of CMOS operational amplifier: including supply current variation

C. Chalk and M. Zwolinski

Indexing terms: Analogue circuits, Testing, Operational amplifiers, SPICE

A SPICE macromodel of a CMOS operational amplifier is described in which the supply current is modelled. This macromodel is suited to multilevel analogue fault simulation. The accuracy of the macromodel is demonstrated by comparison with the full transistor level model. A > 3 times increase in simulation speed compared with the full model is possible.

Introduction: The monitoring of power supply current variation to distinguish between faulty and fault-free operation has been widely described in the testing of digital CMOS circuits and this technique is now being extended to include analogue circuits [1–3]. As no generalised analogue fault model exists, every possible defect must be inserted one at a time into a model of the circuit to determine the effectiveness of a test vector. Each faulty model of the circuit is then simulated using a conventional circuit simulator. The currents drawn by the faulty circuit models are compared with the current drawn by the fault-free model. This can potentially require thousands of hours of computer CPU time.

One solution to this computational difficulty is the use of macromodels to simplify those parts of the circuit not containing any faults, while maintaining the accuracy of the full model. We present a new macromodel of a CMOS operational amplifier that models the power supply current variation. The macromodel is based on those described in [4–7].

The operational amplifier macromodels described in [9, 10] simulate changing supply currents with output load currents but do not accurately model AC and transient supply current variations in VLSI CMOS amplifiers.

We have assessed the accuracy of the macromodel by comparing the slew rate and frequency response of the full transistor-level and the macromodel. We have used two opamp designs for comparison: a simple two-stage amplifier and a cascode amplifier. The simulation times are reduced in both cases, with the cascode opamp providing the best speed up.

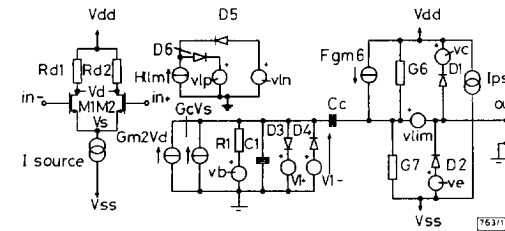


Fig. 1 Macromodel

Macromodel: The macromodel is shown in Fig. 1. In [4–6], the macromodel parameters are taken from performance specifications. We have taken a different approach. The parameters for the components are taken directly from an operating point analysis in SPICE as follows:

The value of $R1$ is derived from the drain-source conductances of the differential input pair and the drain loads. $C1$ is the gate capacitance (C_{gs}) of the output transistors. Components $D3$, $V1+$, $D4$ and $V1-$ have been added to limit $V1$ to $\pm 2V$. (i.e. the large signal voltage levels at the gate of the output transistor). This is necessary to prevent $V1$ increasing to unrealistic levels. Such a situation can occur if there is a large voltage difference between $IN+$ and $IN-$, for a long time relative to the time constant of $C1$ and $R1$.

The derivation of the differential input stage model follows that of [6], and consists of two identical transistor $M1$ and $M2$, load resistors $Rd1$ and $Rd2$, and a current source $Isource$. The gain of this stage is set to unity to avoid extra poles in the frequency response. The transconductances, $Gm1$ and $Gm2$, of these transistors is the same as that of the actual input transistors. SPICE level 1 models are sufficient for these transistors. The width to length ratios are calculated from

$$\frac{W}{L}_{M1,M2} = \frac{Gm2^2}{Isource \cdot Kn} \quad (1)$$

where $Kn = \mu_0 C_{ox}$ is the transconductance parameter in saturation.

To achieve unity gain, the values of $Rd1$ and $Rd2$ are $1/Gm2$. A suitable value for $Isource$ can be measured directly from the operating point analysis or can be derived from the slew rate performance of the opamp as follows:

$$Isource = SlewRate \cdot Cc \quad (2)$$

where Cc is the compensation capacitance shown in Fig. 1. Gc models the common mode rejection ratio (CMRR) [6] and is given by

$$Gc = \frac{1}{(Rd1 \cdot CMRR)} \quad (3)$$

The main component of the AC variation of the power supply current during linear operation is caused by the output stage. In contrast to the voltage-controlled current source and output resistance of [4–6], we have modelled the output stage with a current-controlled current source $Fgm6$, and two output resistances $G6$ and $G7$. $Fgm6$ is controlled by the five currents through vb (small signal gain), vc (output voltage limit positive supply), ve (output voltage limit negative supply), vlp (output current limit positive output swing) and vln (output current limit negative output swing).

Eqn. 4 shows the dependence of the output voltage of the output stage on i_i , the current through vb

$$v_{out} = \frac{Fgm6 \cdot i_i}{G6 + G7} \quad (4)$$

The small signal current gain of $Fgm6$ is derived from the transconductance of the output transistor divided by $R1$. $G6$ and $G7$ are taken directly from the SPICE operating point analysis. The poles and zeros of the output response follow that of [8]. The DC power supply current is modelled by $Ipsu$, a constant current source, with a value derived from the operating point analysis.

We have modelled the large signal characteristics of the output stage by adding voltage and current limiters (two diodes, $D1$ and $D2$, and two voltage sources, vc and ve) as in [4]. Output stage current limiting is similar to that in [7], where a current sensor $vlim$ monitors the current delivered to the load. This controls $Hlim$ and, in turn, vln and vlp control $Fgm6$.

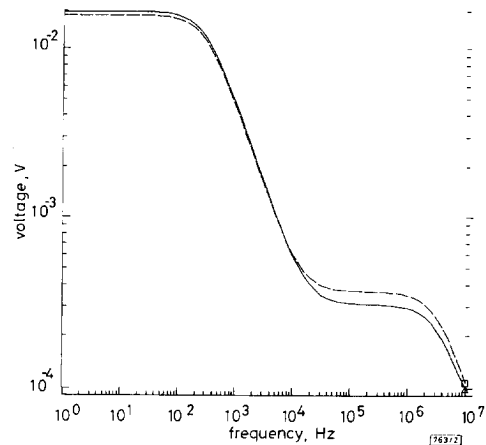


Fig. 2 Open loop frequency response of supply current with 20pF capacitor connected to output

— full-transistor model
 - - - macromodel

Performance: The performance of the macromodel has been compared with the full transistor model. Fig. 2 shows the open loop frequency response of the supply current with a 20pF capacitor connected to the output. Fig. 3 shows the supply current for a transient analysis in which the input signal is switched rapidly to test the slew rate with a capacitive load of 20pF connected to the output. In both examples, the full model is of a two-stage operational amplifier using SPICE level 2 models. The CPU times for a transient analysis using HSPICE on a SPARCstation 1 for the slew rate test are shown in Table 1.

Table 1: CPU times for transient analysis using HSPICE on SPARCstation 1 for slew rate test

Opamp model	Simulation time (transient analysis) [s]
Complete macromodel	9.7
Macromodel without voltage and current limiting	6.6
Transistor-level two-stage opamp model	15.6
Transistor-level cascode opamp model	23.7

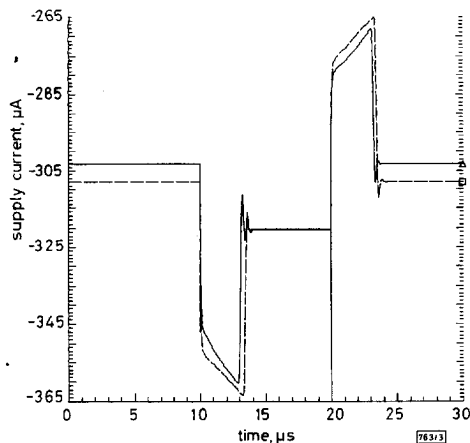


Fig. 3 Supply current for transient analysis in which input signal switched rapidly to test slew rate with 20 pF capacitor connected to output

— full-transistor model
 - - - macromodel

Conclusions: An operational amplifier macromodel for SPICE that incorporates full supply current modelling has been developed. It provides an accurate model for both AC and transient analyses. The model parameters are easily derived from an operating point analysis of the full circuit. If the output voltage and current limiting are removed from the macromodel, a speed-up of up to 3.6 times is achievable with this macromodel, compared with the transistor level model.

© IEE 1995

19 June 1995

Electronics Letters Online No: 19951006

C. Chalk and M. Zwolinski (Department of Electronics and Computer Science, University of Southampton, Southampton SO17 1BJ, United Kingdom)

References

- SUPARJO, B.S., and WILKINS, B.R.: 'Steady state response measurements'. Testing Mixed Signal Circuits, IEE Colloquium 1992/118, May 1992, pp. 2/1-4
- PAPAKOSTAS, D.A., and HATZOPOULOS, A.A.: 'Analogue fault identification based on power supply current spectrum', *Electron. Lett.*, 1993, 29, (1), pp. 118-119
- BELL, I.M., CAMPLIN, D.A., TAYLOR, G.E., and BANNISTER, B.R.: 'Supply current testing of mixed analogue and digital ICs', *Electron. Lett.*, 1991, 27, (17), pp. 1581-1583
- BOYLE, G.A., PEDERSON, D.O., COHN, B.M., and SOLOMON, J.E.: 'Macromodelling of integrated circuit operational amplifiers', *IEEE J. Solid-State Circuits*, 1974, SSC-9, (6), pp. 353-363
- KRAJEWSKA, G., and HOLMES, F.E.: 'Macromodelling of FET/bipolar operational amplifiers', *IEEE J. Solid-State Circuits*, 1979, SSC-14, (6), pp. 1083-1087
- TURCHETTI, C., and MASETTI, G.: 'A macromodel for integrated all-MOS operational amplifiers', *IEEE J. Solid-State Circuits*, 1983, SSC-18, (4), pp. 389-394
- 'Linear circuits operational amplifier macromodels data manual'. Texas Instruments, 1990
- ALLEN, P.E., and HOLBERG, D.R.: 'CMOS analog circuit design' (Harcourt Brace Jovanovich College Publishers, London), pp. 378-379
- ALEXANDER, M., and BOWERS, D.F.: 'Spice-compatible op amp macromodels'. Analog Devices Application Note AN 138, 1990
- BRINSON, M.E., and FAULKNER, D.J.: 'SPICE macromodel for operational amplifier power supply current sensing', *Electron. Lett.*, 1994, 30, pp. 1911-1912

Broadband single-ended to differential signal converter embedded in silicon decision circuit

V. Ramakrishnan, J.N. Albers, R.N. Nottenburg and W.J. Hillery

Indexing terms: Decision circuits, Signal converters

A broadband decision circuit with a novel single-ended input and differential output operating from DC to >6Gbit/s has been fabricated using silicon bipolar transistor technology. Single-ended to differential signal conversion is realised within a single flip-flop stage by using an emitter-coupled feedback loop which eliminates the need for a stable reference voltage source.

Introduction: High speed short haul optical communication links employ decision circuits in receivers to re-align data and to reduce timing jitter caused by laser turn-on delays and skew in optical fibres. Normally, a balanced circuit topology is used in high speed switching circuits to reduce noise and improve the dynamic range. In receiver arrays, crosstalk is a major issue and differential circuitry is essential [1]. Although fully differential optical communication links have been reported, they entail increased complexity, greater power dissipation and suffer from duty cycle distortion at the receiving end because of laser nonlinearities [2]. Hence, the majority of communication regenerators use single-ended optoelectronic converters/preamplifiers followed by limiting or AGC amplifiers. A reference voltage is generated on-chip or applied externally to ensure balanced operation of the succeeding stages [3]. We demonstrate unbalanced-to-balanced signal conversion within a master-slave flip-flop using a new technique. This decision circuit may be used to retime digital data from single-ended preamplifiers, from DC to several gigabits per second, thereby offering the advantages of differential circuit operation without the need for a reference voltage or coupling capacitors.

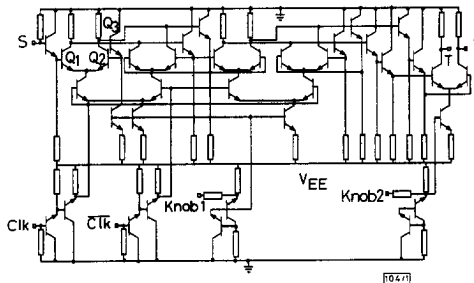


Fig. 1 Schematic diagram of decision circuit with embedded single-to-differential signal converter

Circuit design and fabrication: The decision circuit (Fig. 1) is a master-slave flip-flop using series gated transistor switches. The input signal is applied to the base of Q1. A complementary signal is derived from the collector of Q1 and coupled to the base of Q2 via Q3. Previously reported feedback ECL (FECL) switches in which the base of Q2 is directly connected to the collector of Q1 have been developed [4] to realise large switching gains for small signal swings by using positive feedback. However, the bandwidth was limited [5] by the large capacitive load at the collector of Q1 and the saturation of Q1 and Q2. We have introduced Q3 into the FECL loop to provide a low impedance complementary signal source for Q2 and to buffer the collector of Q1, which is advantageous in low power circuits in which the load resistance is >150Ω. Q3 improves the bandwidth performance without changing the nature of the voltage transfer characteristic and ensures that Q1 and Q2 are never saturated. The effective differential input voltage swing is the sum of the single-ended input voltage and collector voltage swing of Q1. This improves the input dynamic range over that of a current switch with one input connected to a reference voltage. The circuit was designed to operate from a single -5V supply. The data and clock inputs are terminated to ground using 50Ω on-chip resistors for impedance matching. The output is