

Programmable Time-Multiplexed Switched-Capacitor Variable Equalizer for Arbitrary Frequency Response Realizations

R. Pérez-Aloe, J. F. Duque-Carrillo, E. Sánchez-Sinencio, J. M. Valverde, G. Torelli, A. H. Reyes, and F. Maloberti

Abstract— A time-multiplexed digitally-programmable switched-capacitor (SC) variable equalizer which allows the realization of arbitrary frequency responses is presented. The circuit performs the same operation as a cascade of N second-order programmable equalizers, where N is also the multiplexing order. Except for the storing capacitors, the rest of the circuitry is shared for all individual equalizer functions (channels), resulting in silicon area savings higher than 60% with respect to a direct circuit implementation for $N = 4$. The impact on circuit performance of crosstalk effects is discussed. Experimental results of a 3-V timesharing SC equalizer architecture fabricated in a CMOS 1.2 μm technology are given for different values of the multiplexing order. The circuit has been designed to be incorporated in a programmable hearing aid device.

Index Terms—MOS analog integrated circuits, programmable filters, sampled data filters, switched capacitor filters, time division multiplexing.

I. INTRODUCTION

SWITCHED-CAPACITOR (SC) filtering is a very well established technique to process signals mainly in the audio frequency range. Advantages such as the insensitivity of the response to the unavoidable process fabrication deviations, as well as the possibility of having a digital control over their characteristics, constitute two of the stronger points of these kinds of circuits.

Today there is an increasing demand for circuits able to meet low power consumption and low silicon area requirements, especially for portable battery-operated systems with room constraints. In some systems, even area and power savings can become more important design targets than an extremely high performance, although the loss in the performance has not been excessive. Conventional design approaches of SC filters require a number of amplifiers which are proportional to the order of the realized transfer function and, in the case of high-order programmable SC filters, can be very expensive in terms of silicon area due to the capacitor banks that control the response. Because of their ability to relax power and area requirements, considerable attention has been paid to timesharing or multiplexing techniques for the implementation of either high-order SC filters [1]–[7] or SC filter banks [8],

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[9]. Some of the proposed timesharing schemes for high-order filters [1]–[4] use a single amplifier per pole pair, achieving a reduction by a factor of two in the amplifier count. Other proposed multiplexing circuits [5] reduce by a factor of N the number of amplifiers required to implement an arbitrary N th-order filter function using state space synthesis techniques, although some storage element is needed to perform multiplexing. Other interesting timesharing approaches implement a cascade of biquadratic SC cells with just two op-amps [6] or by sequentially computing the individual outputs of the cascade [7].

In this work, prompted by the necessity of having available an economical structure in terms of area and power and, simultaneously, a high degree of flexibility to implement any arbitrary frequency response with reasonable accuracy, a time-multiplexed scheme of a digitally-programmable SC bump equalizer is introduced. The time-shared circuit performs as N series-connected second-order programmable equalizers, where N is also the multiplexing order. The responses of the individual equalizers are computed sequentially and the only set of capacitor arrays required is dynamically reconfigured according to the programming bits stored in a memory register.

II. PROGRAMMABLE TIME-MULTIPLEXED SC EQUALIZER ARCHITECTURE

Any frequency response can be realized with a cascade of N second-order programmable magnitude equalizers (BE_i), as illustrated in the block diagram of Fig. 1, provided that N is large enough. The general equalizer structure is programmable in the central frequency (f_{oi}), gain (A_i) at the central frequency and bandwidth (BW_i) of each section. The complete transfer function of the cascade will be given by the product of the N individual second-order equalizer transfer functions [10], as the following expression indicates

$$H(s) = \frac{V_{\text{out}}(s)}{V_{\text{in}}(s)} = \prod_{i=1}^N \frac{s^2 + A_i BW_i s + \omega_{oi}^2}{s^2 + BW_i s + \omega_{oi}^2} \quad (1)$$

where the bandwidth is defined as $BW_i = \omega_{oi}/Q_i$. Obviously, the higher the flexibility required to fit more precisely any frequency response shape is, the larger the number of cascaded second-order sections is, and therefore, power and area consumptions become progressively more unacceptable for micropower systems with room constraints.

The sampled-data nature of SC circuits, as well as the possibility of being programmable with a digital word, can be exploited to implement the transfer function of (1) in a time-multiplexed way. Fig. 2 shows the conceptual diagram of the time-multiplexed system along with the associated

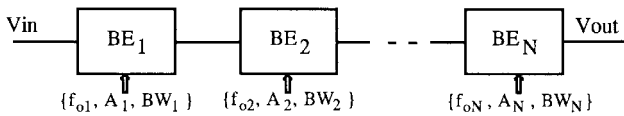
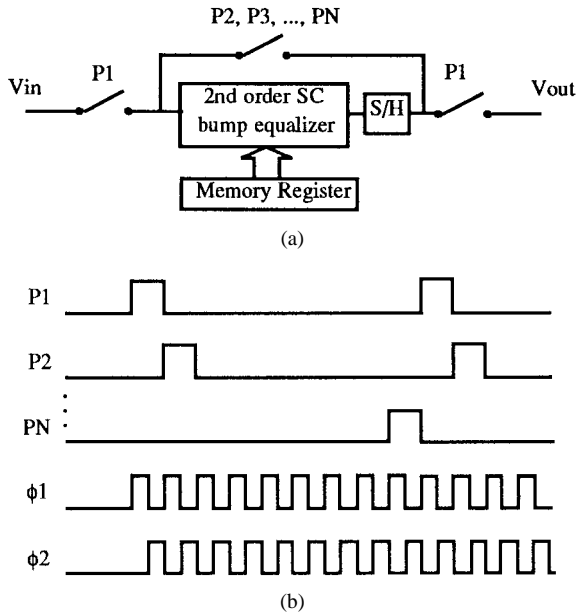

 Fig. 1. A cascade of N second-order programmable variable equalizers.


Fig. 2. (a) Block diagram of the time-multiplexed system and (b) clock waveforms.

clock waveforms. The bump equalizer section works with nonoverlapping clock phases ϕ_1 and ϕ_2 . The operation of the system is as follows. At the clock period P_1 , the input signal is sampled and the multiplexed circuit is configured to act as the first equalizer BE_1 . The output of BE_1 is computed, stored, and fed back to the cell input in the next clock period P_2 . At the beginning of this period P_2 , the time-multiplexed equalizer is configured to perform the operation of BE_2 . The capacitor banks are dynamically reprogrammed according to the corresponding memory registers contents during the small delays existing between the rising edges of the clock pulses P_i and ϕ_1 . The successive equalizer responses are computed sequentially and, at the end of the next clock period P_1 , the output sample corresponding to the complete equalization cascade is available, achieving a considerable silicon area saving with respect to the nonmultiplexed scheme shown in Fig. 1. The fact that an output sample is available at the end of next clock period P_1 depends, of course, on the particular type of processing carried out in the bump equalizer and sample-and-hold (S/H) circuits, as will be shown below.

In regard to power consumption, it is clear that the proposed multiplexed solution of Fig. 2 divides by N the number of amplifiers that otherwise would be required. However, the effective clock period available for slewing plus settling is also divided by N and, hence, the amplifiers have to be designed with higher performance (larger gain-bandwidth product and slew-rate) if the same transfer charge accuracy is to be maintained. As a consequence, larger current consumption and transistor aspect ratios are required with respect to a

nonmultiplexed solution and, therefore, we can conclude that amplifier power and area consumptions are not so greatly reduced as the remaining circuitry area.

Fig. 3 shows the circuit schematic of our time-multiplexed second-order SC bump equalizer. Every capacitor array enclosed in a square box indicates a capacitor array that is dynamically reconfigured in the way explained above. The multiplexed circuit has been designed to perform, at most, with a multiplexing order of four, but the extension of the operation to higher multiplexing orders does not introduce any conceptual difference. Notice that the architecture of Fig. 3 uses a fully differential (FD) topology but, for simplicity reasons, one half of the circuitry, as well as the switches that disconnect the capacitors C_A and C_{oi} from the virtual ground amplifiers terminals when they are inactive, have been omitted. In the same circuit schematic of Fig. 3, the basic SC bump equalizer architecture [11] is highlighted with a thicker line. The bump equalizer incorporates an SC integrator with low area requirements [12], although other SC integrator structures can be used as well. The operation principle of this SC integrator consists of taking advantage of the integrator idle phase to attenuate the signal so that the time-constant is determined by the product of two capacitor ratios. The capacitance spread is reduced by a factor of B , where B equals $1 + C_D/C_A$. The z -domain equalizer transfer function is given by the following expression:

$$H(z) = \frac{V_{out}^o(z)}{V_{in}^o(z)} = - \frac{z^2 + z \left(\frac{C_w^2}{C_o^2} \frac{1}{B^2} + \frac{C_Q C_k}{C_s C_o} \frac{1}{B} - 2 \right) + \left(1 - \frac{C_Q C_k}{C_s C_o} \frac{1}{B} \right)}{z^2 + z \left(\frac{C_w^2}{C_o^2} \frac{1}{B^2} + \frac{C_Q}{C_o} \frac{1}{B} - 2 \right) + \left(1 - \frac{C_Q}{C_o} \frac{1}{B} \right)} \quad (2)$$

The equalizer parameters $f_o \cong (C_w f_c)/(2\pi C_o B)$, $A \cong C_k/C_s$, $BW \cong (C_Q f_c)/(2\pi C_o B)$, where f_c represents the sampling frequency, can be independently programmed by means of the capacitor arrays C_w , C_k , and C_Q , respectively. An outstanding feature of the basic SC bump equalizer used from the time-multiplexing point of view consists in that every programming capacitor bank in the integrators corresponds to an input capacitor rather than an integrating capacitor. Thus, any capacitor bank can be reconfigured from one channel to another without any loss of information, since the output voltage samples of each integrator are stored in the feedback capacitors until the next clock period P_i .

The S/H cell used in the time-multiplexed circuit corresponds to the structure reported in [13]. This FD S/H circuit samples the equalizer output during ϕ_1 , holds the signal during ϕ_2 , and either feeds it back to the cell input at the next phase ϕ_1 if the clock period P_i is different from P_1 , or provides a valid output sample otherwise.

Since in the general second-order variable equalizer structure (see highlighted portion of Fig. 3), the input signal is injected into three different nodes, corresponding to the low-pass (LP), band-pass (BP) and high-pass (HP) paths, some of these basic functions can be obtained in a particular clock period P_i with the general multiplexed scheme of Fig. 3 by

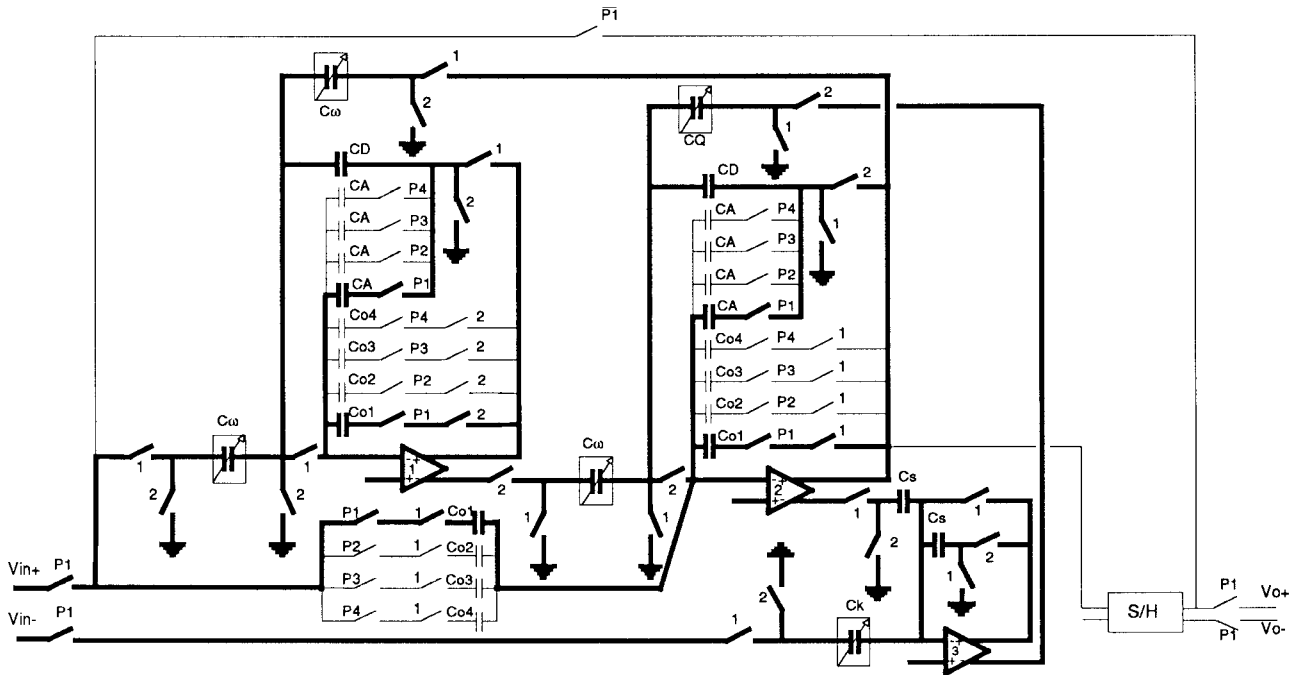


Fig. 3. Time-multiplexed digitally programmable SC variable equalizer with maximum multiplexing order of four.

proper values of the programming bits. Thus, to perform the operation of an HP filter, it is enough to program the capacitor array C_ω connected to the input and the array C_k for zero capacitance value during the corresponding period P_i . However, in order to have this possibility available through the programming bits, the corresponding capacitor arrays must be implemented without any fixed capacitor in the bank, which reduces the maximum area savings achievable. In our design, the circuit of Fig. 3 can perform the operation of an HP filter followed by a cascade of three bump equalizers. The HP filter operation is achieved by eliminating the corresponding signal paths during P_1 by means of two additional switches not shown in the general structure of Fig. 3.

As pointed out above, the SC integrator used in the equalizer reduces the capacitance spread by a factor of B , however, the input-referred amplifier offset voltage is increased by the same amount. It can be demonstrated [11] that the total dc offset at the equalizer output (V_{os}) is only influenced by the offset voltage (V_{off1}) of amplifier 1. The reason why the offset voltages of amplifiers 2 and 3 do not contribute to the total offset voltage can be found in the fact that the resulting transfer functions from the inputs of these amplifiers to the output correspond to high-pass and band-pass responses, respectively, and therefore, are eliminated for $z = 1$ ($\omega = 0$). In the case of the time-multiplexed implementation, this dc voltage is propagated and added to the different individual equalizer contributions. Thus, the general expression which provides the output dc offset as a function of the multiplexing order can be easily derived, obtaining

$$V_{os} = \sum_{i=1}^N (-1)^{N+1} \left(2 + \frac{C_D}{C_{\omega, p_i}} \right) V_{off1} \quad (3)$$

where C_{ω, p_i} accounts for the capacitance value C_ω at the generic clock period P_i . The exponential term $(-1)^{N+1}$ arises

as a consequence of the sign inversion that takes place in the equalizer transfer function of (2). A tradeoff solution has been adopted between reduction in capacitive spread and increase in offset voltage.

III. CROSSTALK EFFECTS

There are several potential mechanisms associated with the operation of the time-shared circuit of Fig. 3 which can lead to some loss of accuracy. Some of these effects arise from the leakage currents that discharge the hold capacitors of the S/H circuit, as well as the integrating capacitors, while the corresponding channels are inactive. The use of large capacitor values and minimum sized transistor switches reduces the leakage effect, however, the resulting time constants are limited by the sampling period available.

Nonetheless, the more important cause of loss of accuracy is due to the crosstalk mechanisms among channels originated by some parasitic capacitances that couple the individual equalizer operations. The crosstalk effect caused by the parasitic capacitances associated with the virtual ground nodes of the amplifiers can be neglected if the open-loop gain is designed large enough. However, the strongest impact is introduced by the parasitic capacitance C_p that couples input and output amplifier terminals as Fig. 4 shows. This capacitance causes some charge loss at the instants when the integrating capacitors C_{oi} are connected, since the stored charge must be shared with the parasitic capacitance, reducing the amplifier output voltage. Fig. 5 illustrates the impact on the circuit of Fig. 3 of the crosstalk effect for different values of C_p . As can be observed, the simulated operation of the time-multiplexed equalizer is an HP filter cascaded with a variable equalizer, which means a multiplexing order of two. With a proper circuit layout, this crosstalk capacitance can be kept to a minimum

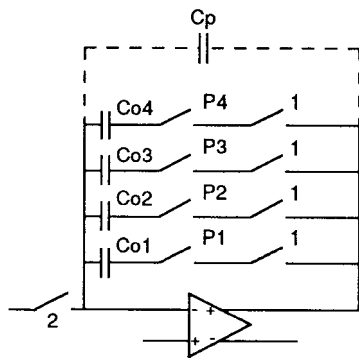


Fig. 4. A time-shared SC integrator showing the crosstalk parasitic capacitance C_p .

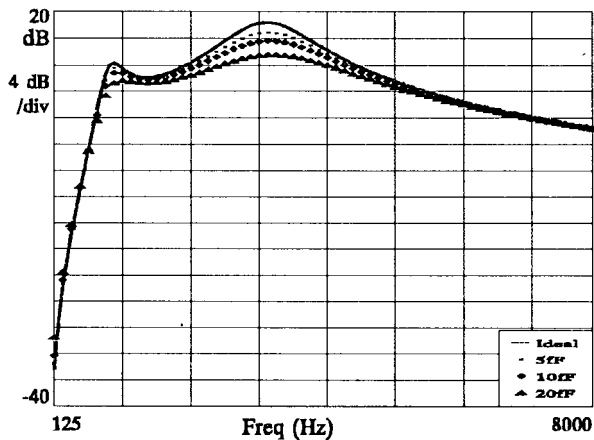


Fig. 5. Simulated results illustrating the crosstalk effect for different parasitic capacitance values C_p ($N = 2$).

value. Moreover, in [4], a design solution has been proposed for partial compensation of this crosstalk effect in FD SC circuits, but it requires an extra clock phase and slightly more complicated hardware.

IV. EXPERIMENTAL RESULTS

The programmable time-multiplexed bump equalizer has been designed and fabricated in a $1.2\text{-}\mu\text{m}$ n-well double-poly double-metal CMOS process (Fig. 6). The circuit occupies $2.7 \times 1.3 \text{ mm}^2$, including some test blocks that allow the possibility of observing the different channel responses separately. It has been designed to operate with 3 V of total supply voltage and 50 kHz of effective sampling frequency (ϕ_1, ϕ_2) per channel. The amplifier incorporated consists of an FD folded-cascode structure with an internal feedback loop based on resistive degeneration of current mirrors [15] to carry out the required output common-mode component stabilization. The capacitor banks have been implemented as 3-b binary-weighted arrays. Therefore, any equalization channel can provide up to 512 different frequency responses, and the number of possible responses of the time-multiplexed equalizer, for $N = 4$, results almost unlimited. The silicon area savings achieved is around 60% with respect to the nonmultiplexed implementation.

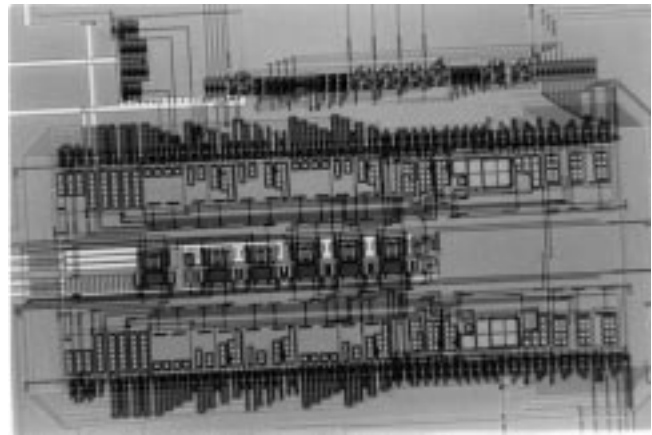


Fig. 6. Chip photomicrograph.

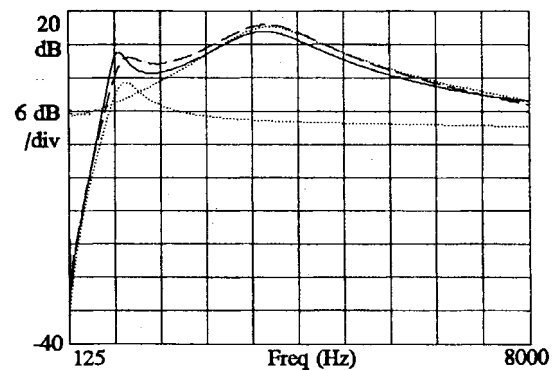


Fig. 7. An experimental circuit response ($N = 2$) equivalent to an HP filter followed by an equalizer (dotted curves: measured individual channel responses, dashed curve: ideal product of channel responses, solid curve: measured response of the complete circuit).

Fig. 7 shows an experimental frequency response of the time-multiplexed equalizer operating with a multiplexing order of two, which corresponds to the simulated response of Fig. 5. In the same plot, the measured individual responses of both channels (dotted curves) along with the ideal product of them (dashed curve) are also shown. We have estimated the total parasitic capacitance C_p in our design, resulting in a value approximately equal to 2.4 fF. As observed in Fig. 7, the maximum deviation (approximately 2 dB) between the ideal and the experimental multiplexed (solid curve) responses agrees well with the simulated results shown in Fig. 5, confirming this crosstalk mechanism as the main error source in the time-multiplexed scheme.

The current design has been carried out to be incorporated in a programmable hearing aid device as the cell responsible for frequency response correction. Thus, the resulting hearing aid circuit shows an almost unlimited capability for precise hearing loss compensation regardless of shape and, simultaneously, a very economical implementation mainly in terms of silicon area. For this hearing loss compensation purpose, we found that an appropriate time-multiplexed circuit operation consists of programming the system to act as a cascade composed by an HP filter followed by three series-connected variable equalizers as indicated above. Every channel of the time-shared circuit sweeps well-defined frequency range within the

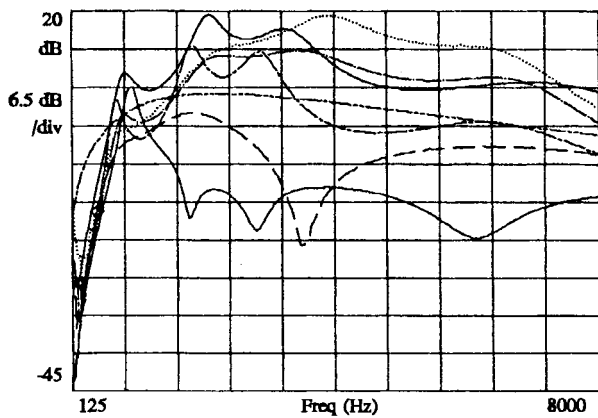


Fig. 8. Selected measured frequency responses with a multiplexing order of four.

TABLE I
PROGRAMMABILITY RANGES OF DIFFERENT PARAMETERS

	f_0 (kHz)	A_0 (dB)	BW (kHz)
HP	(.1, 1)	(0, 18)	(.125, 1.5)
BE ₁	(0.25, 2)	(-14, 20)	(0.25, 3.5)
BE ₂	(0.5, 3)	(-14, 20)	(0.5, 7)
BE ₃	(3, 6.5)	(-14, 20)	(3.5, 15)

audio band of interest [125 Hz, 8 kHz]. The programmability ranges of the different parameters are shown in Table I for 200 kHz of total clock frequency. In order to illustrate the versatility of the time-multiplexed circuit, Fig. 8 shows several experimental frequency responses corresponding to different settings of programming bits. In practice, the programming bit setting for the best frequency response fitting of the time-multiplexed equalizer is determined with the help of a computer routine based on the downhill simplex method [16].

The total harmonic distortion (THD) measured for different amplitudes of a 1-kHz input sinewave is plotted in Fig. 9. THD remains below 1% up to $1.8V_{pp}$ differential input signal. For the distortion measurements, the individual equalizers were programmed with the flattest response which provides a total gain of approximately 4 dB at a frequency of 1 kHz. The input-referred noise integrated over the frequency band [125 Hz, 8 kHz] is $0.19 \text{ mV}_{\text{rms}}$. Combining these figures, a dynamic range higher than 70 dB results. The measured total current consumption is $62 \mu\text{A}$.

V. CONCLUSION

A multiplexing technique for the realization of arbitrary frequency responses with very low silicon area requirements has been presented. The circuit consists of a time-shared SC magnitude-equalizer that performs the same operation as a cascade of digitally-programmable equalizers. The full programmability is achieved by means of only one set of capacitor arrays, which is dynamically reconfigured according the programming bits. Crosstalk errors caused by input-output parasitic capacitances in the amplifiers are the main accuracy limitation of the technique. In our circuit, the maximum deviation between measured and ideal simulated responses was smaller than 2 dB for $N = 2$. Experimental results obtained from a CMOS test-chip prototype with a maximum

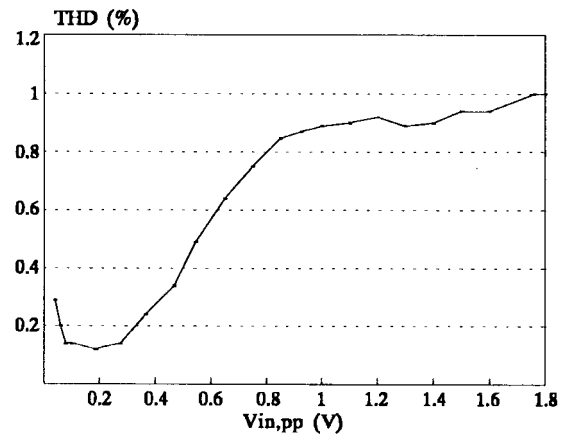


Fig. 9. THD for different input amplitude values ($f_{in} = 1 \text{ kHz}$).

multiplexing order of four have demonstrated the potentiality of the proposed circuit.

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