

# Continuous-Time Filters from 0.1Hz to 2.0GHz

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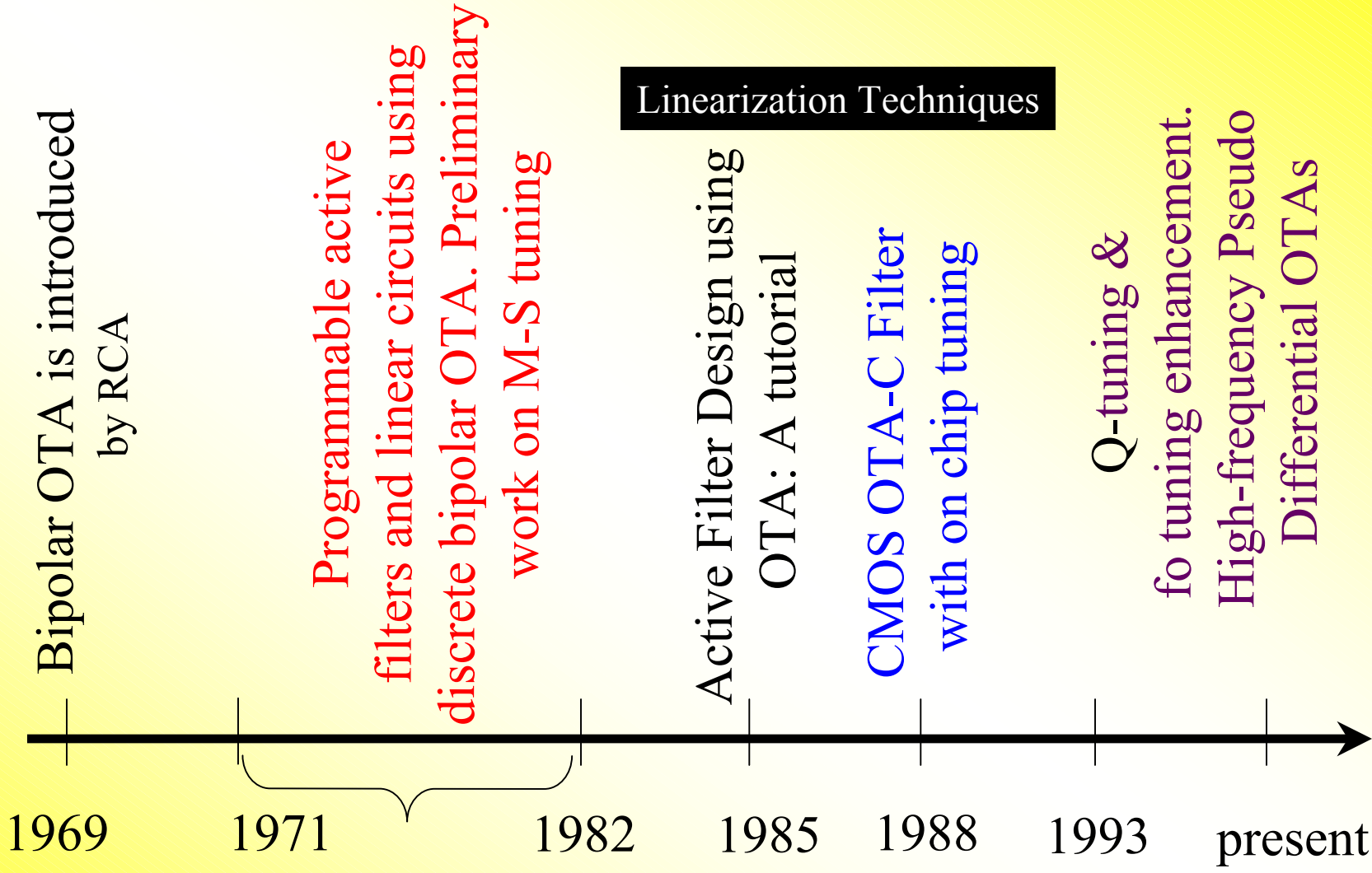
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**Abstract.**-The bipolar transconductance amplifier (OTA) was commercially introduced in 1969 by RCA. Designers began using OTAs in the middle 80's, since then the CMOS-OTA has becoming a vital component in a number of electronic circuits, both in open loop and in closed loop applications. Here, we will focus on open loop applications. Continuous-time filters implemented with transconductance amplifiers and capacitors known as Gm-C or OTA-C are very popular for a host of applications. These applications involve frequency of operation from a few tents of a hertz up to several gigahertz. Several of those applications are in medical electronics and seismic area where the frequency range is between 0.1Hz up to 20Hz. Other applications in the audio range do not commonly use OTA-C filters because switched-capacitor techniques excel in this range. But for frequency range of a few MHz like in Intermediate Frequency (IF) filters in RF receivers OTA-C implementations are very attractive. For a few GHz range applications where the OTA becomes a simple differential pair there is number of researchers investigating LC-oscillators and filters. In this tutorial we discuss practical implementations of transconductance amplifiers oriented for wide range of applications for example in medical, IF filters, hard disk drive linear phase filters, LC-oscillators and RF filters. Furthermore the unavoidable tuning scheme to compensate the Gm/C deviations due to process technology variations is discussed. OTA single ended, fully differential and pseudo differential versions are introduced together with the common-mode feedback circuits needed for proper operation of differential architectures.

# Continuous-Time Filters from 0.1Hz to 2.0GHz

## Outline.-

- **Introduction and Motivation**
- **A family of Transconductance for different frequency ranges (applications).**
- **Common-mode feedforward and feedback strategies needed for differential output filters.**
- **Frequency- and Q-tuning techniques for OTA-C filters**



# Evolution of the OTA

# Typical applications of OTA-C filters and frequency ranges

Applications

- **Medical**
- **Seismic**
- **Built-in generators**

- **Hard disk drivers filters**
- **XDSL**
- **Sigma-delta ADC**
- **IF Receiver filters**

**RF Filters & oscillators**

0.1

1

$10^1$

$10^2$

$10^6$

$10^7$

$10^8$

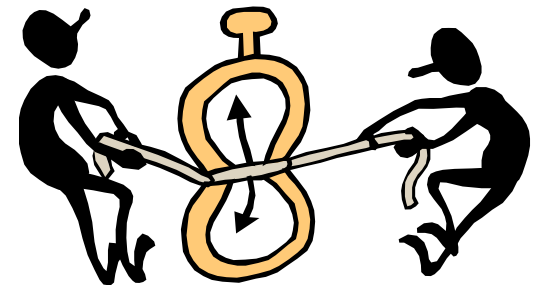
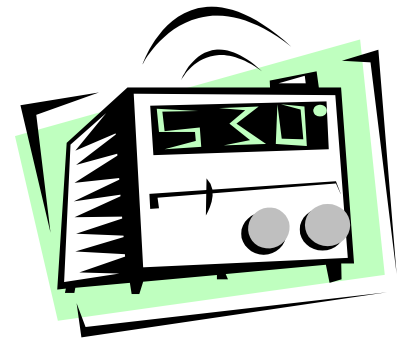
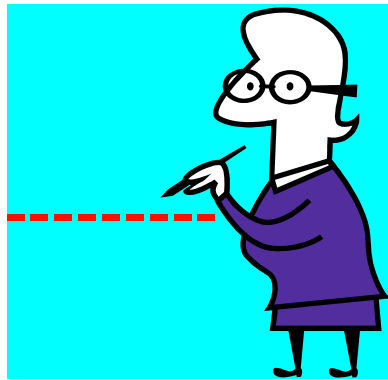
$10^9$



Frequency (Hz)



# A few examples of continuous-time filters in a host of applications



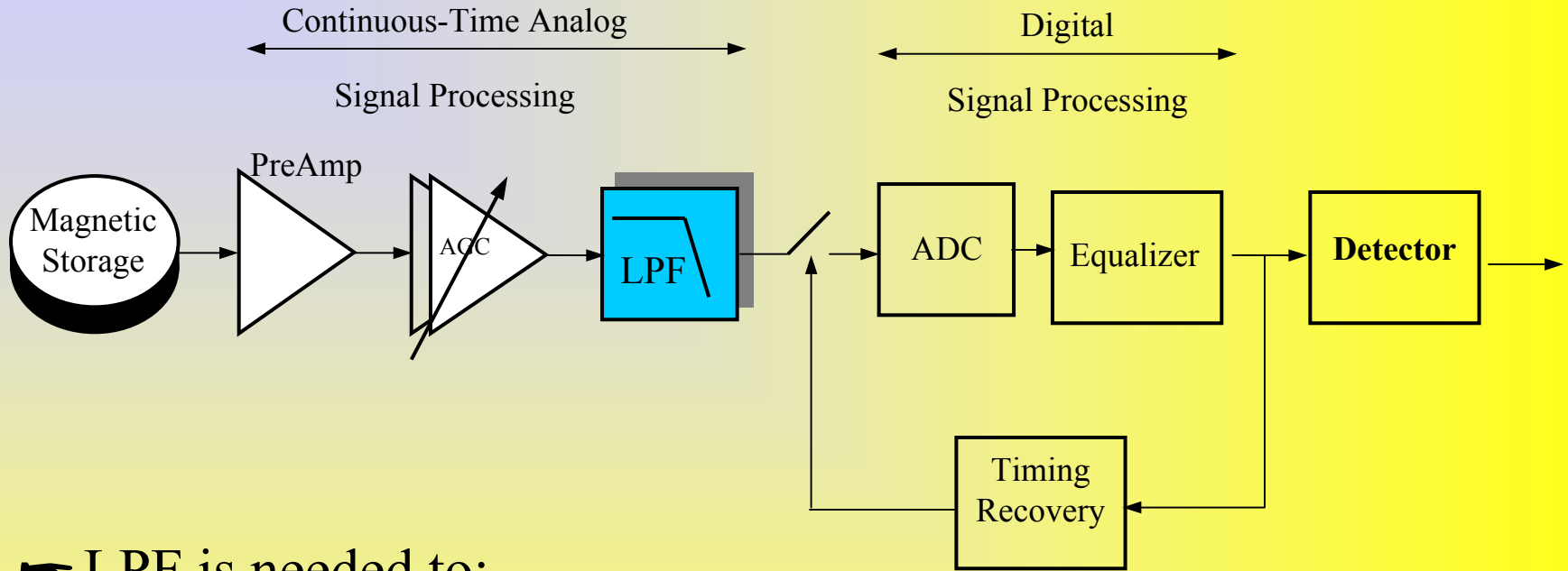
# Applications for continuous time filters



Top view of a 36 GB, 10,000 RPM, IBM SCSI server hard disk, with its top cover removed.

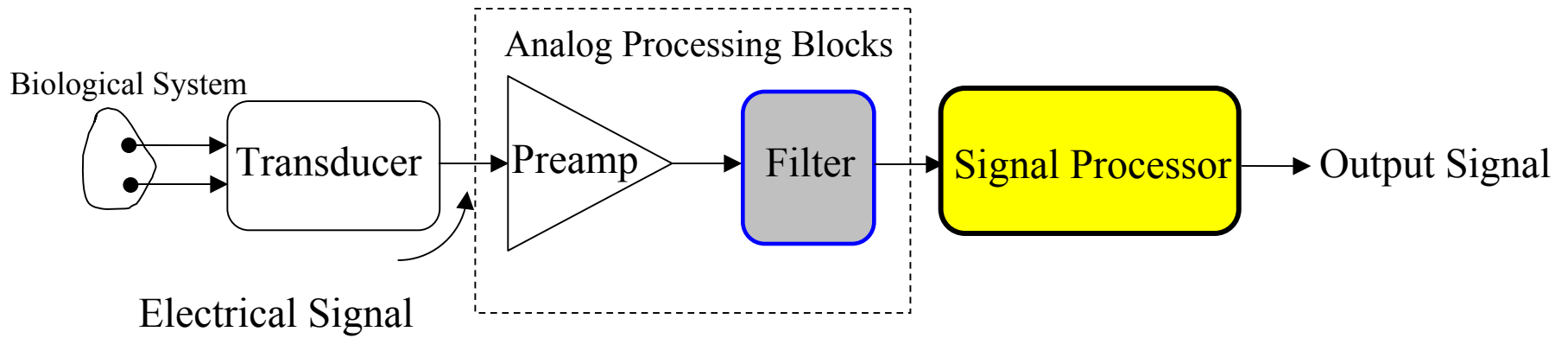
Read channel of disk drives --  
for phase equalization and  
smoothing the wave form

# Hard Disk Driver Read Channel

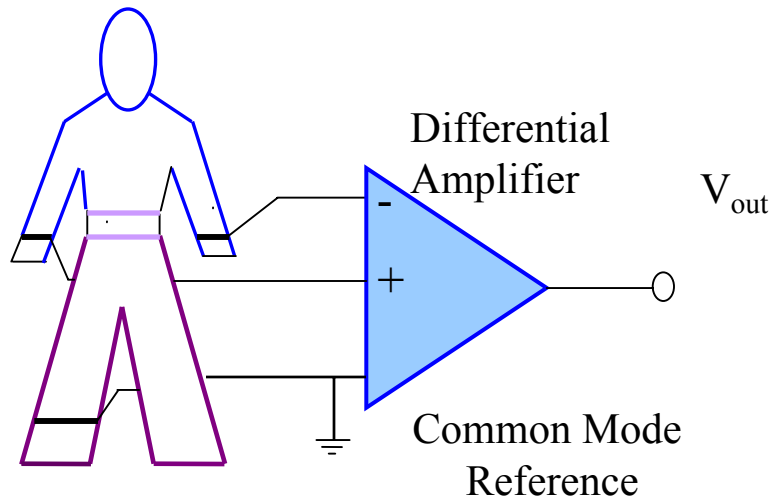


➡ LPF is needed to:

- ➡ Limit signal and noise bandwidth;
- ➡ Provide anti-aliasing prior to sampling;
- ➡ Provide significant contribution to overall equalization.



**Block Diagram of a general purpose bioelectric signal acquisition system.**

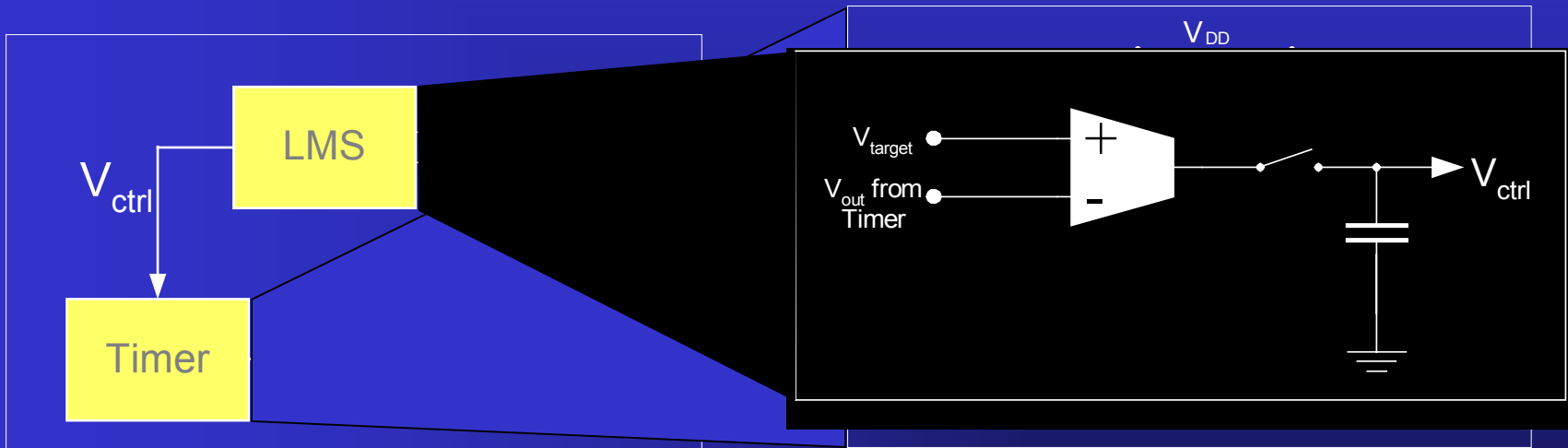


Parameter	Typical range
Gain	1-1000
Bandwidth	0.1 Hz-10KHz
Dynamic Range (DR)	60dB-100dB
CMRR	80-140dB
$Z_{input}$	10M $\Omega$ -1G $\Omega$ at 60Hz
$V_{noise}$	$<10\text{nV}/\sqrt{\text{Hz}}$
$I_{noise}$	$<1\text{[A]}/\sqrt{\text{Hz}}$

Typical configuration for the measurement of bio-potentials

# Continuous-Time Linear Ramp Implementation

## LMS Integrator



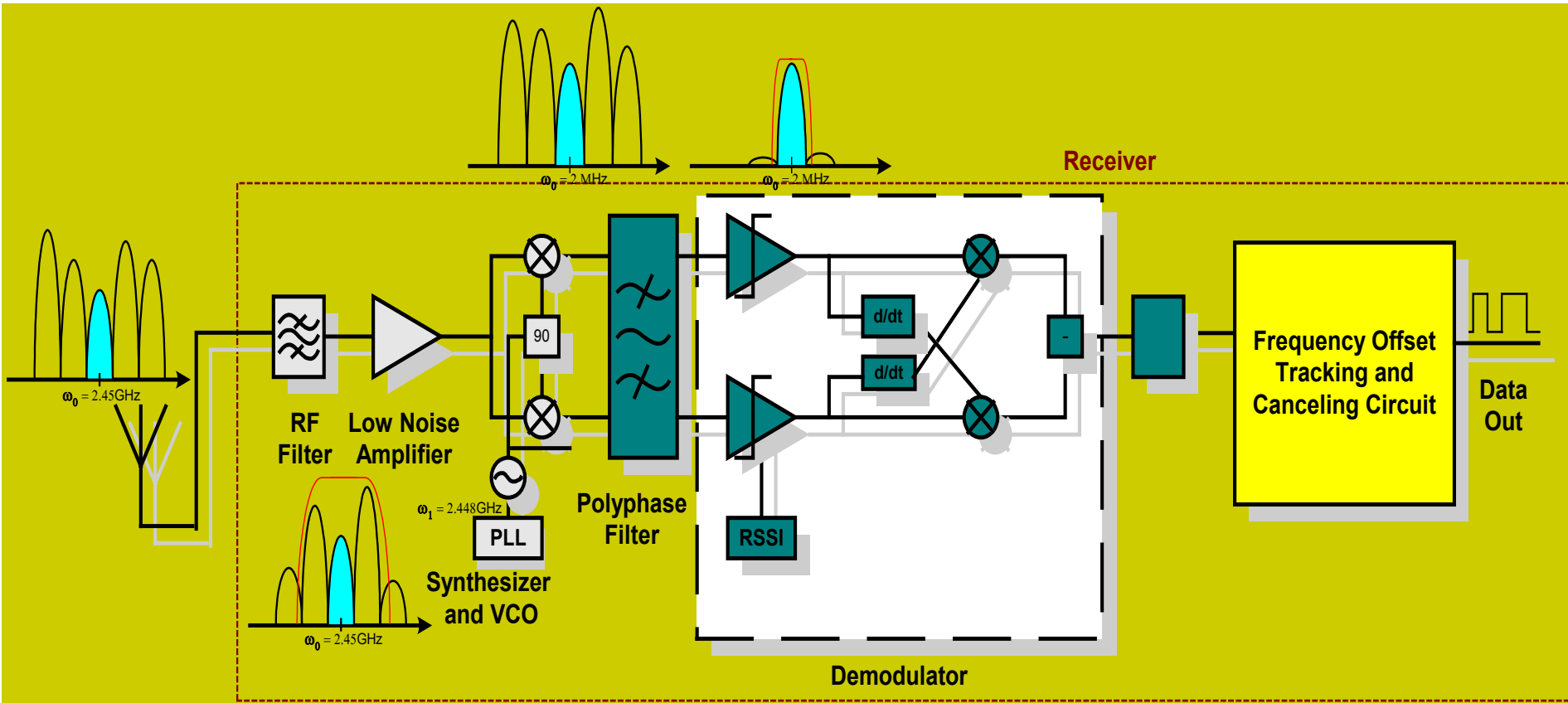
- The Timer is a cascode current source with  $V_{ctrl}$  controlling the gate voltage of the current source transistor
- The LMS block is an OTA-C integrator with a switch to control the charging of the capacitor



Receivers and Transmitters in wireless applications -- used in PLL and for image rejection

6185i digital cell phone from Nokia.

# Low-IF Bluetooth Receiver



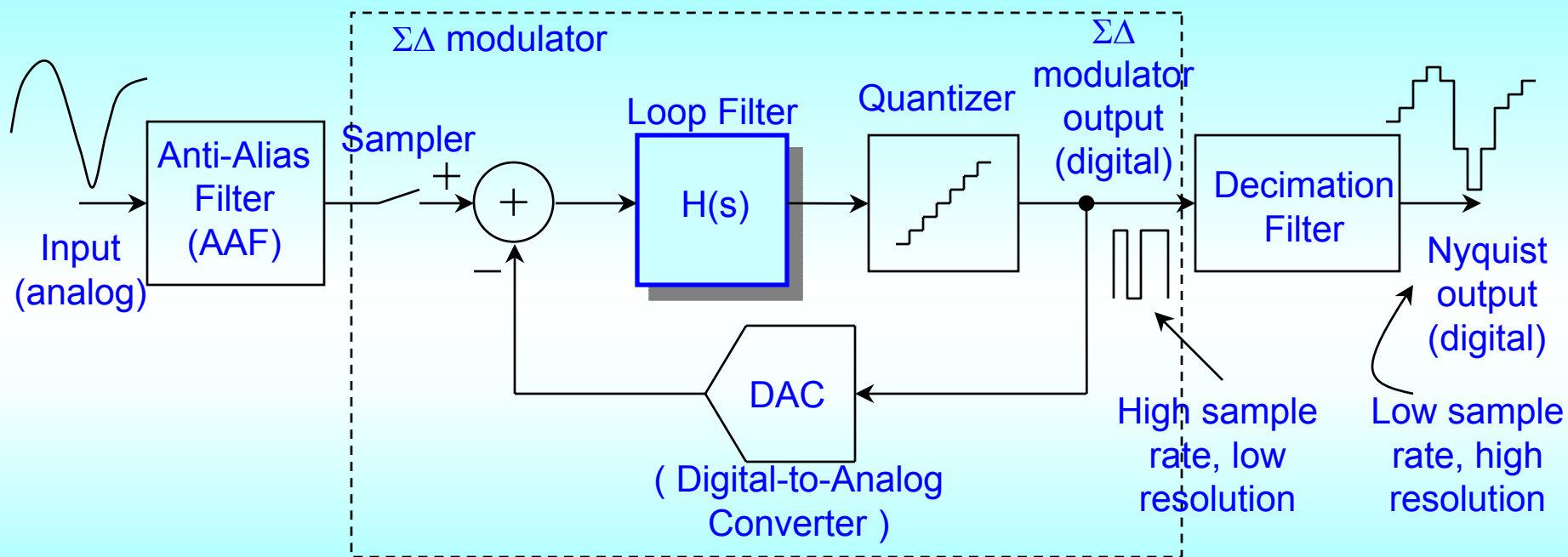
- Active polyphase filter is used to reject image and select channel.



CMP-35 portable MP3 player

All multi media applications --Anti aliasing before ADC and smoothing after DAC.  
Filters in the Sigma-Delta Converters

# Sigma-Delta Oversampled A/D Conversion

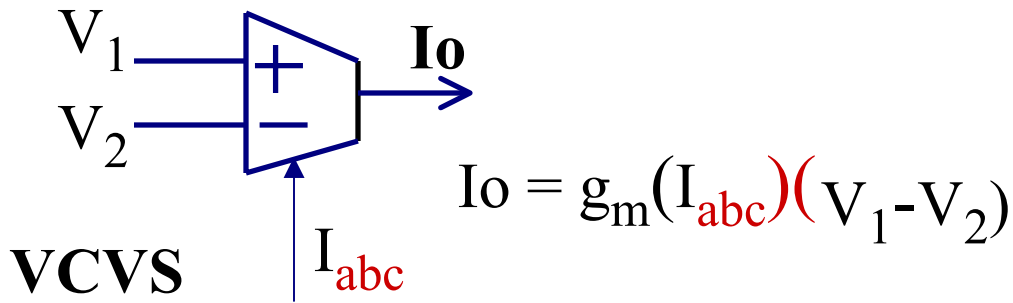


Functional level diagram of a general continuous-time sigma-delta oversampled analog-to-digital converter

**A family of Transconductances for different  
frequency ranges applications.**

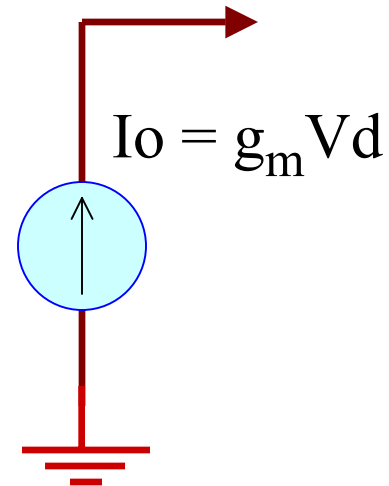
# OPERATIONAL TRANSCONDUCTANCE AMPLIFIER (OTA)

First commercial OTA produced by RCA in 1969, i.e., CA3080



$$\frac{V_1}{V_2} +$$

$$\frac{V_d}{V_2} -$$



The transconductance gain “ $g_m$ ” is a function of the  $I_{abc}$ .

$$g_m = h_1 I_{abc} \quad \text{for bipolar and weak inversion MOSFETs}$$

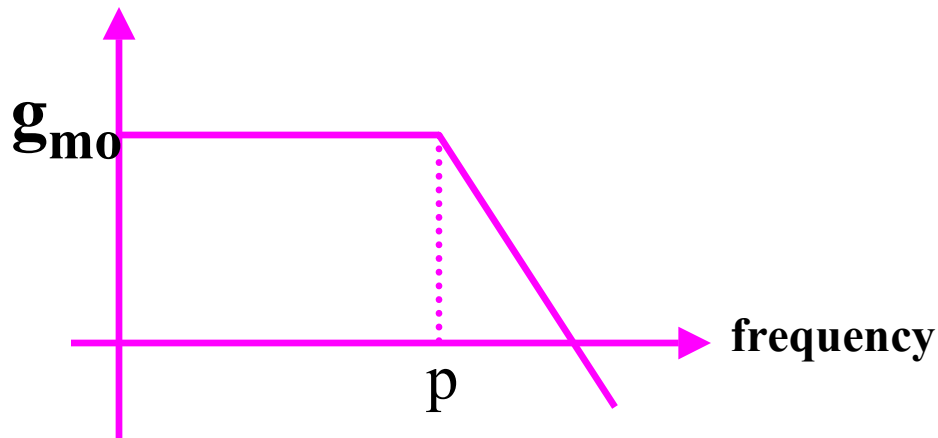
$$g_m = h_2 [I_{abc}]^{1/2} \quad \text{for MOSFETs in saturation}$$

# OPERATIONAL TRANSCONDUCTANCE AMPLIFIER (OTA) Frequency Dependence

$$G_m = g_{m0} / (1 + s/p)$$

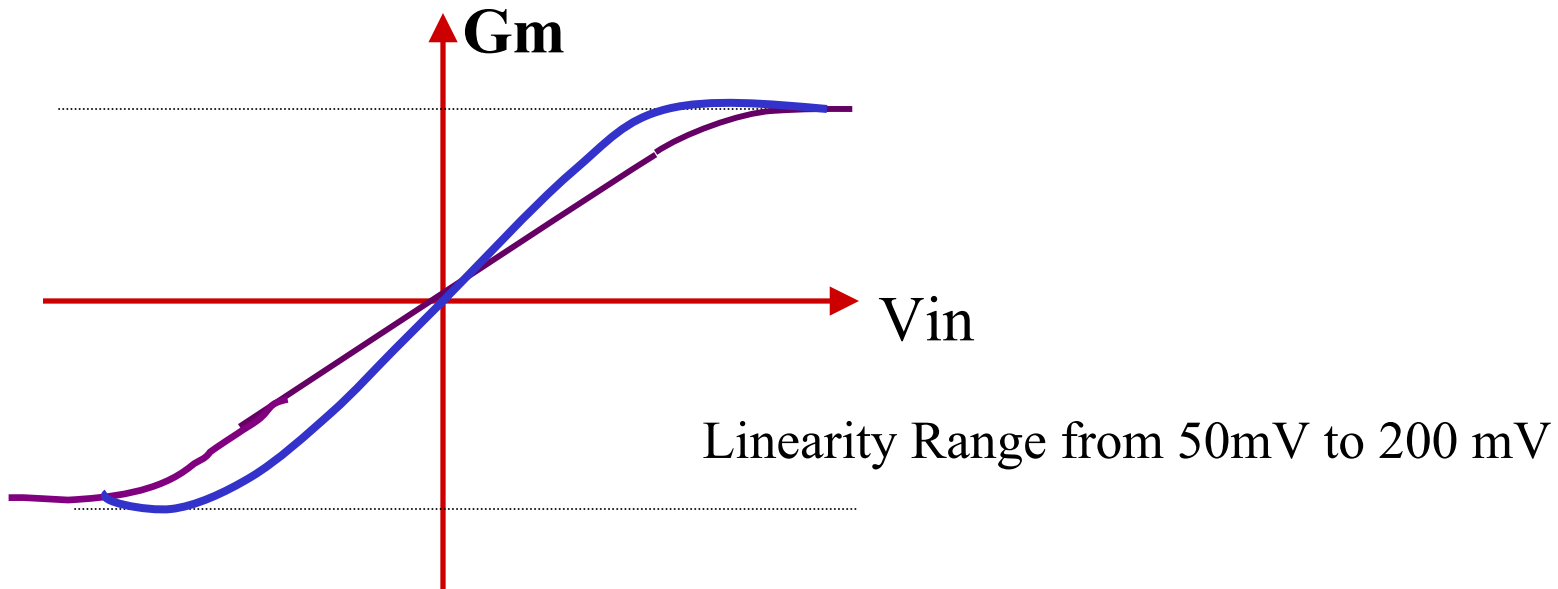
Where  $g_{m0}$  is the DC transconductance gain

$p$  is the dominant pole which is around 10MHz to 100Mhz



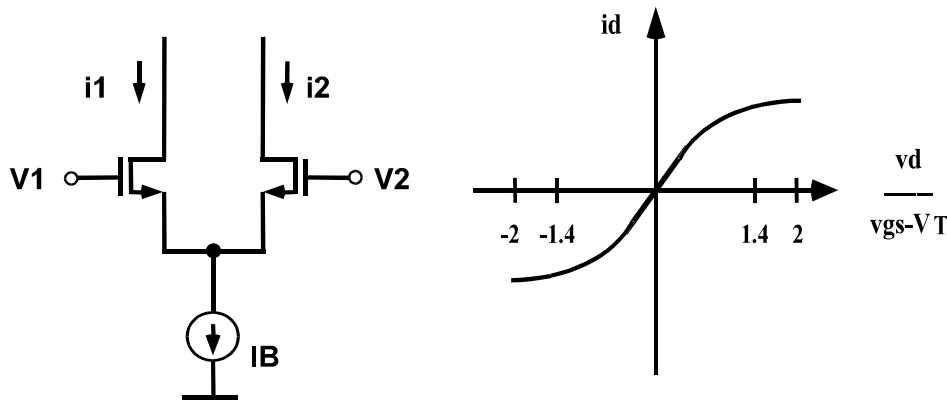
## Issues about the OTA:

- Operated in open loop conditions
- High-Frequency Operation
- Poor Linearity Range



# Linearity Issues:

## Differential Pair as a V-I converter



$$i_d = \left( \frac{\sqrt{2\beta_1 I_B}}{2} \right) v_d \sqrt{1 - \left( \frac{v_{in}}{2(v_{GS} - v_T)} \right)^2}$$

$$g_m = \sqrt{2\beta_1 I_B}$$

$$HD2 = 0$$

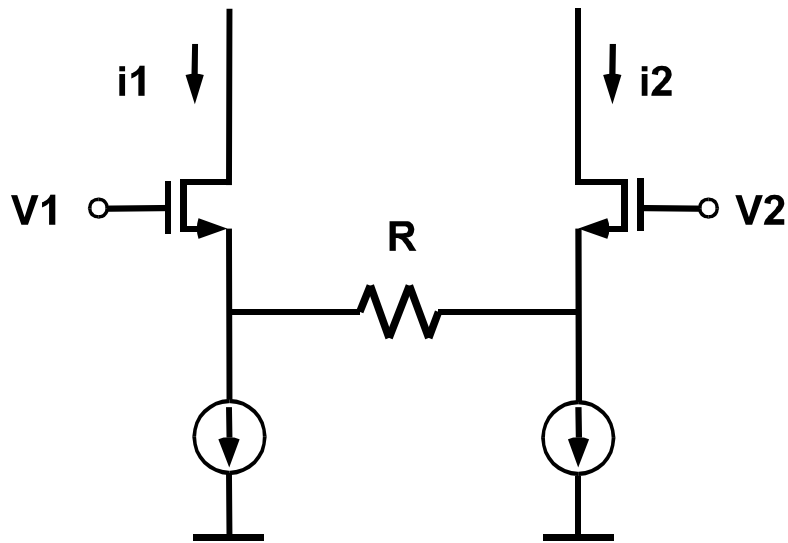
$$HD3 = \frac{1}{32} \left( \frac{v_d}{2(v_{GS} - v_T)} \right)^2$$

How to improve the linearity ?



# Differential Pair with Source Degeneration

## Improved linearity



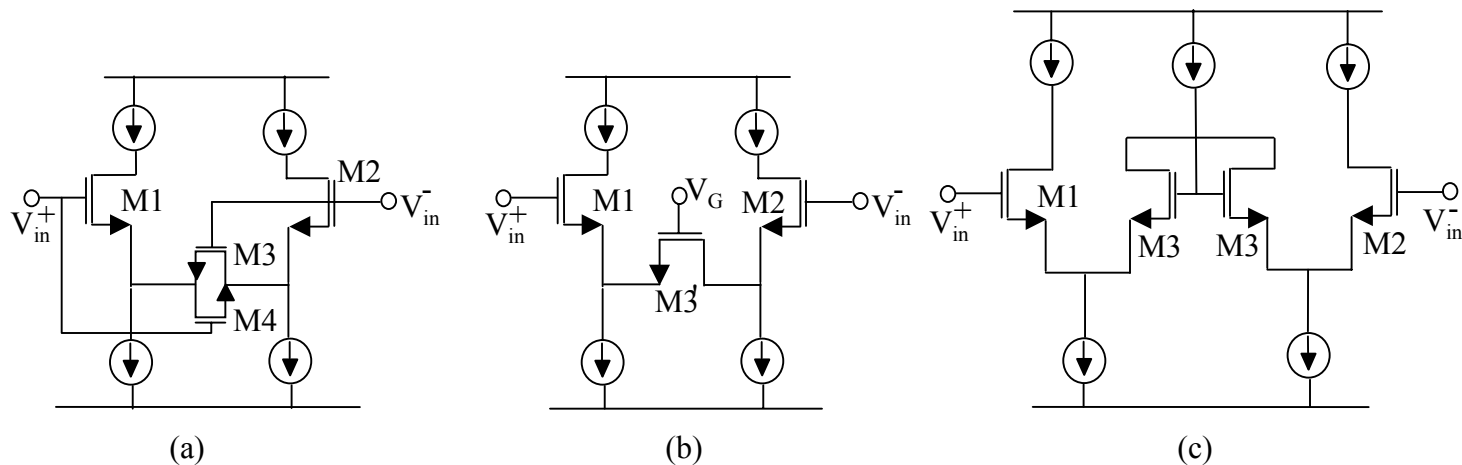
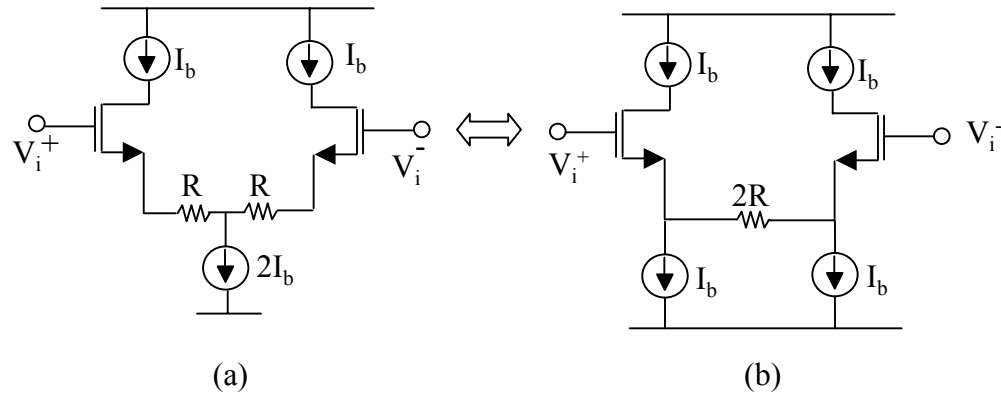
$$1/n = \frac{1}{1 + g_m R}$$

$$i_d = \left( \frac{\sqrt{2\beta_1 I_B}}{2} \right) \frac{v_d}{n} \sqrt{1 - \left( \frac{v_{in}}{2n(v_{GS} - v_T)} \right)^2}$$

$$HD2 = 0 \quad \text{Ideally}$$

$$HD3 = \frac{1}{32n^2} \frac{v_{in}^2}{(v_{GS} - v_T)^2}$$

# $g_m$ linearization schemes via **source degeneration**.

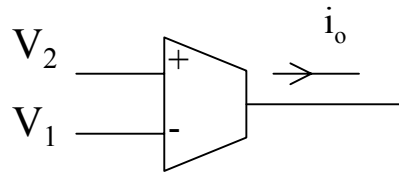


Active Source Degeneration topologies; (a) and (b) transistors biased on triode region and (c) with saturated transistors.

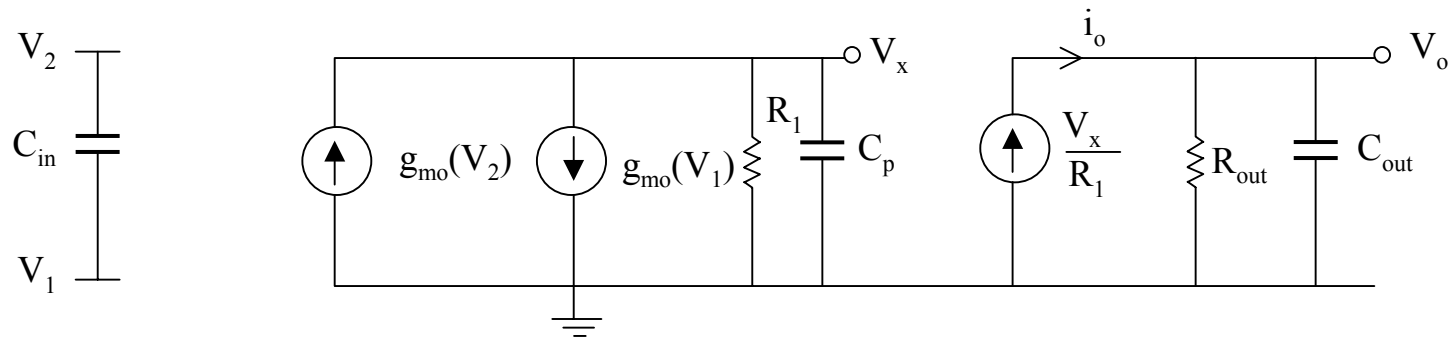
Table 3. Properties of OTAs using source degeneration

Reference/Figure	Transconductance	Properties
Fig. (a)	$\frac{g_{m1}}{1 + \frac{\beta_1}{4\beta_3}}$	Low sensitive to common-mode input signals. The linear range is limited to $V_{in} < V_{DSAT}$ , and THD=-50 dB. M1=M2, M3=M4
Fig. (b)	$\frac{g_{m1}}{1 + g_{m1}R}$ $R = 1/\mu_o C_{ox}(V_{gs} - V_T)$	Highly sensitive to common-mode input signals. For better linearity large $V_{GS3}$ voltages are required. Large tuning range if $V_G$ is used.
Fig. (c)	$\frac{g_{m1}}{1 + g_{m1}/g_{m3}}$ <p style="text-align: center;">M1=M2</p>	Low sensitive to common-mode input signals. Limited linearity improvement, HD3 reduces by -12 dB. More silicon area is required.

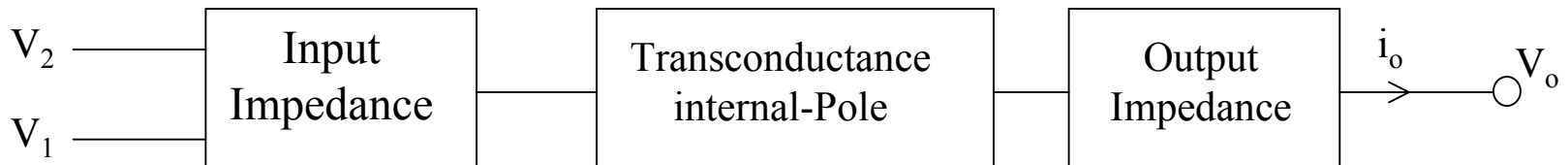
# A Linear CMOS OTA Macromodel



$$g_m = \frac{g_{mo}}{1 + \frac{s}{\omega_p}} \quad ; \quad \omega_p = \frac{1}{R_1 C_p}$$

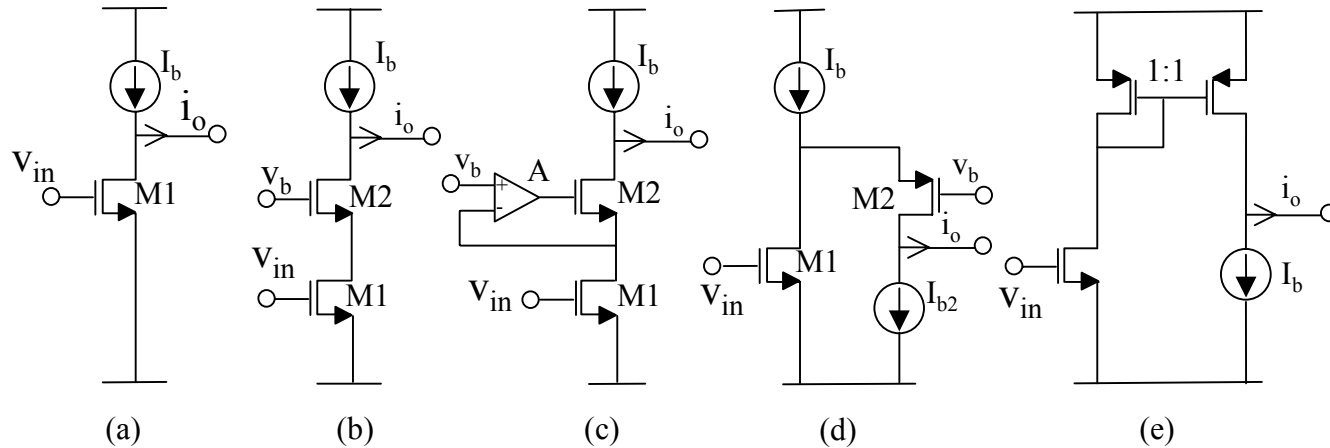


Real OTA Macromodel



OTA Macromodel Representation

# Single-input Transconductor (ST) Implementations



Single Input (a) Negative Simple Transconductor, (b) Cascode Transconductor, (c) Enhanced Transconductor, (d) Folded-Cascode Transconductor, (e) Positive Simple Transconductor.

- Observe that:

$g_m = f(I_b)$ , the exact relation is a function of the transistor region of operation.

- Note that output impedance of (a) and (e) are only  $1/g_{ds}$  and (b), (c) and (d) implementations have larger output impedances.

## Properties of Simple (single input/ single output) Transconductors

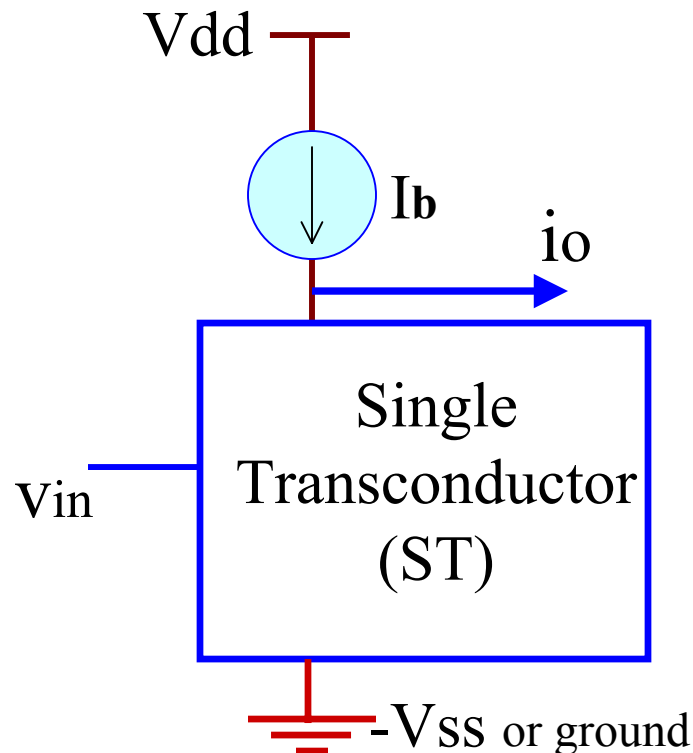
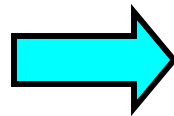
Structure/ Figure	$R_{out}$	Min $V_{DD}$ *
Simple/1(a)	$\frac{1}{g_{ds1}}$	$\sqrt{\frac{2I_B}{k}} + V_{sat,I_B}$
Cascode/1(b)	$\frac{g_{m2}}{g_{ds1} g_{ds2}}$	$(1+m)\sqrt{\frac{2I_B}{k}} + V_{sat,I_B}$
Enhanced/1(c)	$\frac{A g_{m2}}{g_{ds1} g_{ds2}}$	$(1+m)\sqrt{\frac{2I_B}{k}} + V_{sat,I_B}$
Folded/1(d)	$\frac{g_{m2}}{g_{ds1} g_{ds2}}$	$\sqrt{\frac{2I_B}{k}} + V_{Tp} + V_{sat,I_B}$

\* The bottom devices of the cascode pairs have an aspect ratio of  $(W/L)_1/(W/L)_2=m^2$ .  $k$  is a technological parameter determined by the mobility, and the gate oxide;  $V_{sat,I_B}$  is the saturation voltage for the  $I_B$  current source.

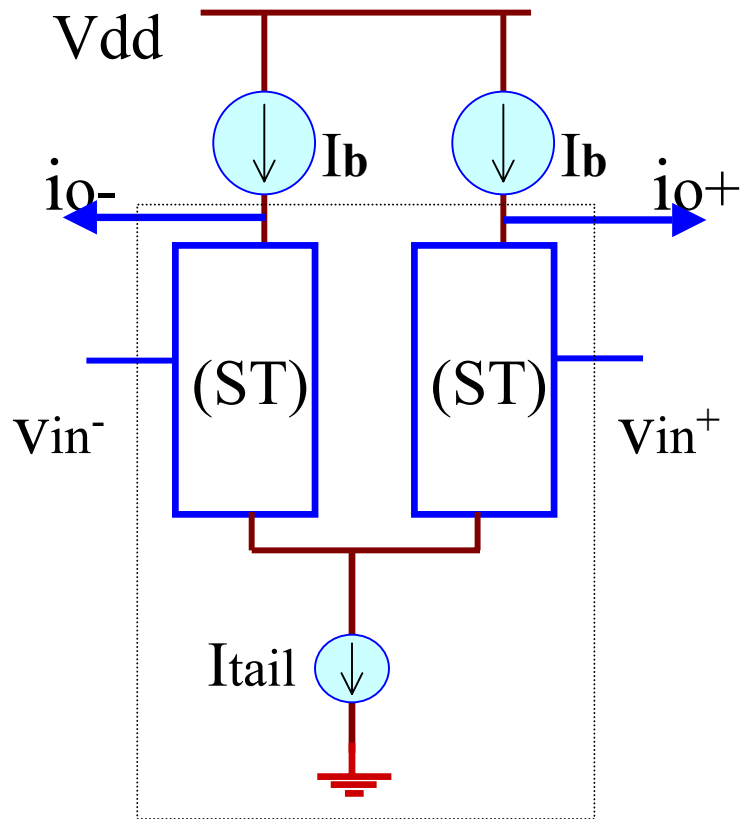
Based on the simple (single input) transconductance how can one generate differential input/single output and fully differential transconductances?



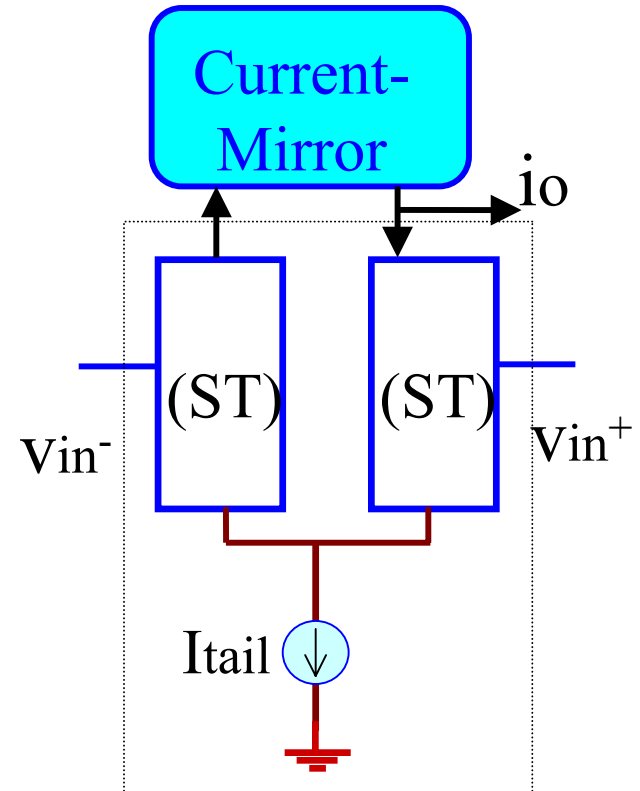
Basic Building Block



## Two possible implementations of OTAs

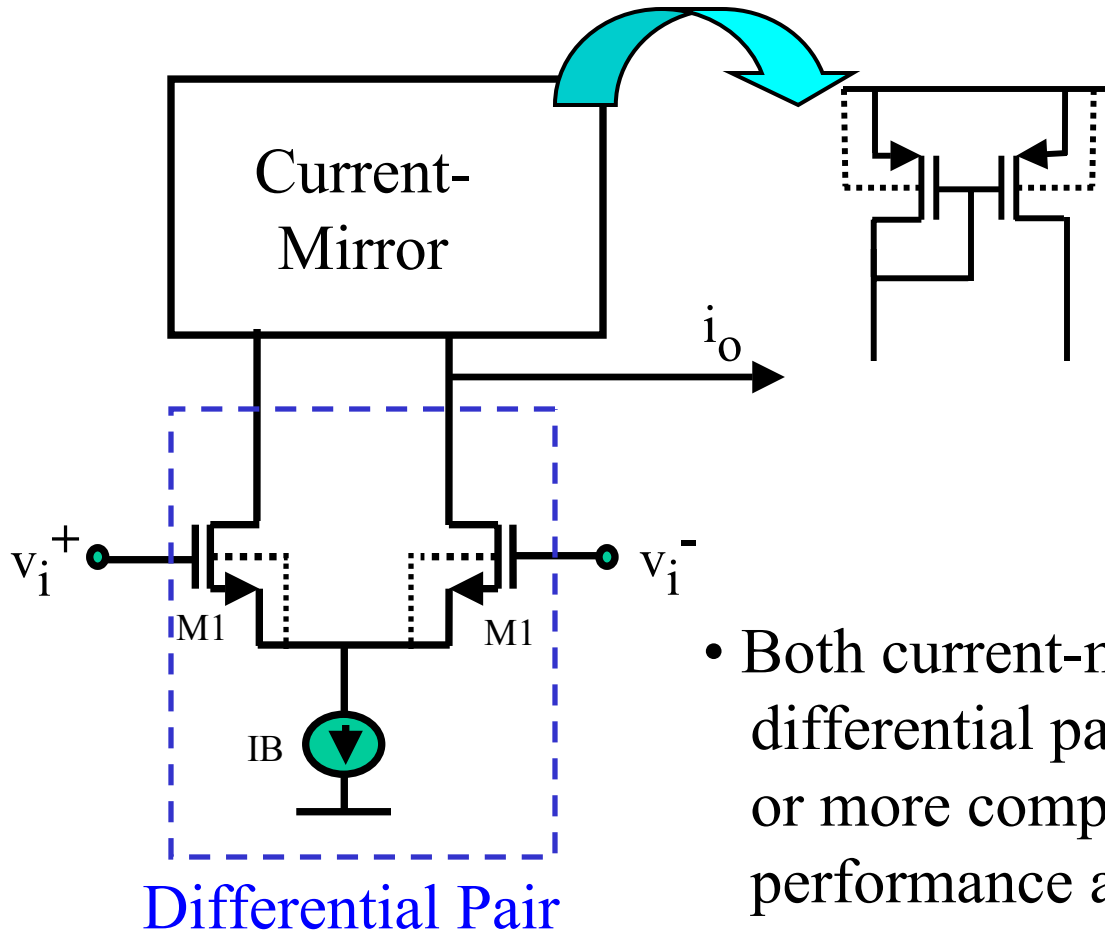


Differential Input -  
Differential Output



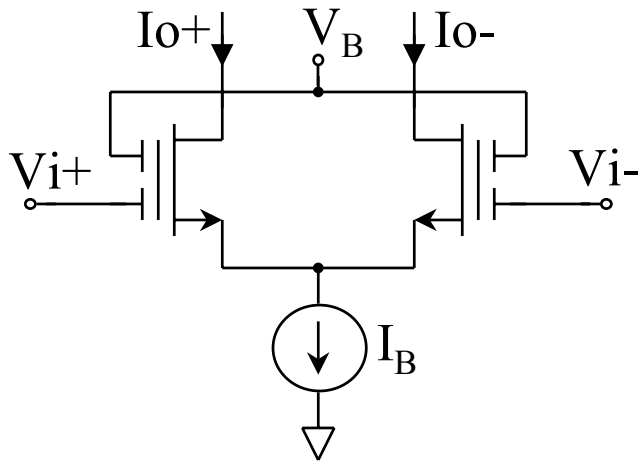
Differential Input -  
Single-ended Output

# Basic Differential Transconductance (Single-ended)

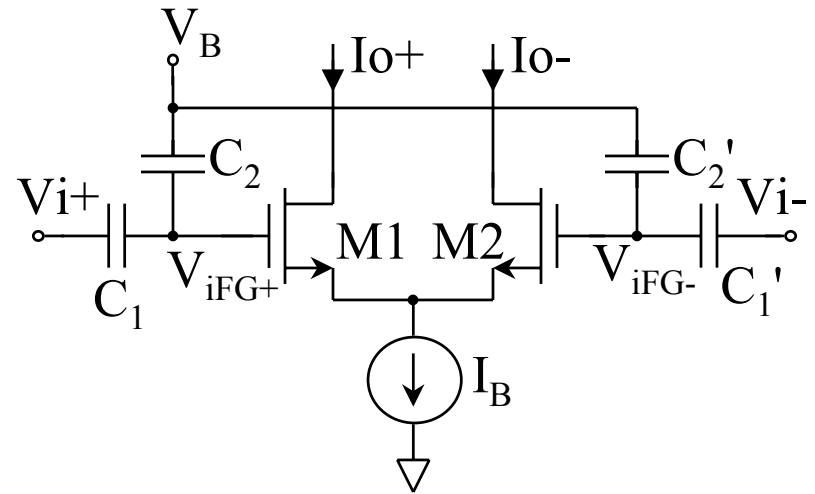


- Both current-mirror and/or differential pair can be simple or more complex to improve performance and/or to increase design tradeoffs

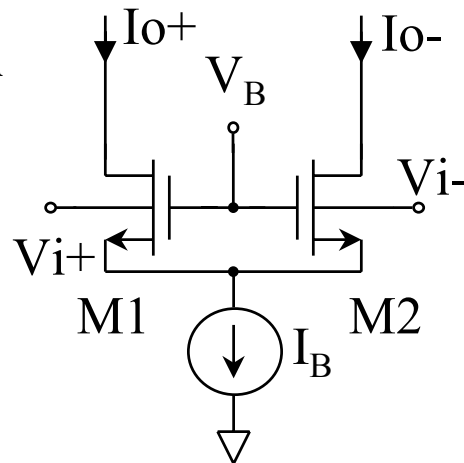
# Potential Solutions for Rail-to-Rail Amplifiers: OTAs suitable for Low Frequency Applications



**FG DP Implementation**

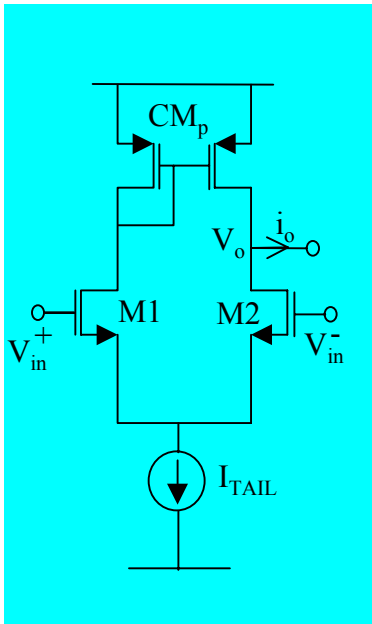
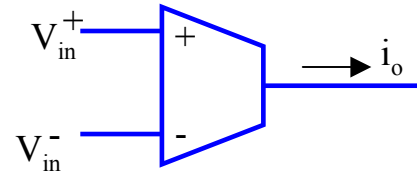


**FG DP Equivalent circuit**

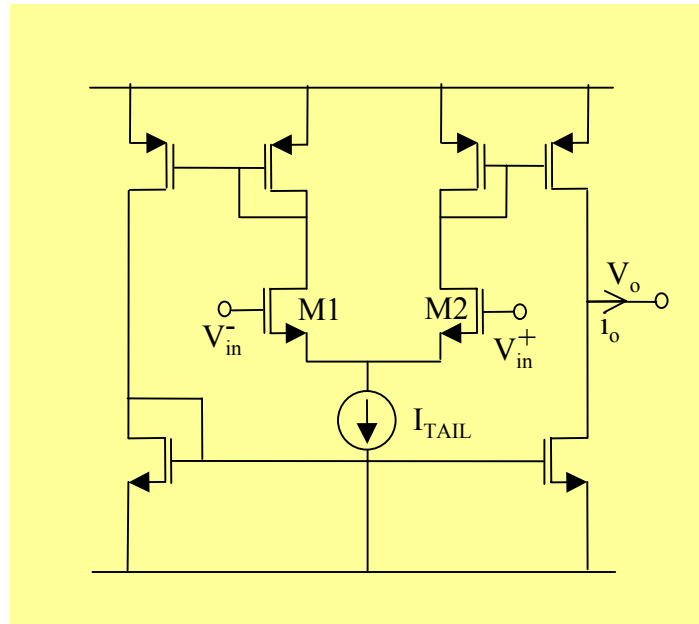


**Bulk Driven DP**

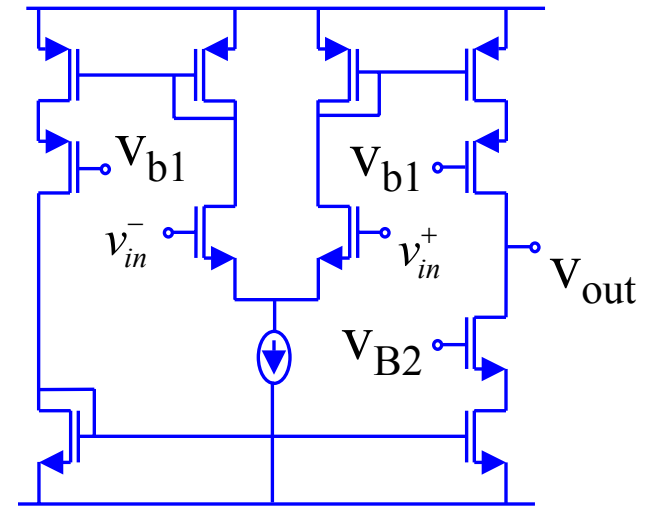
# Three Conventional Differential Input –Single Ended OTAs



(a) Simple differential input OTA.

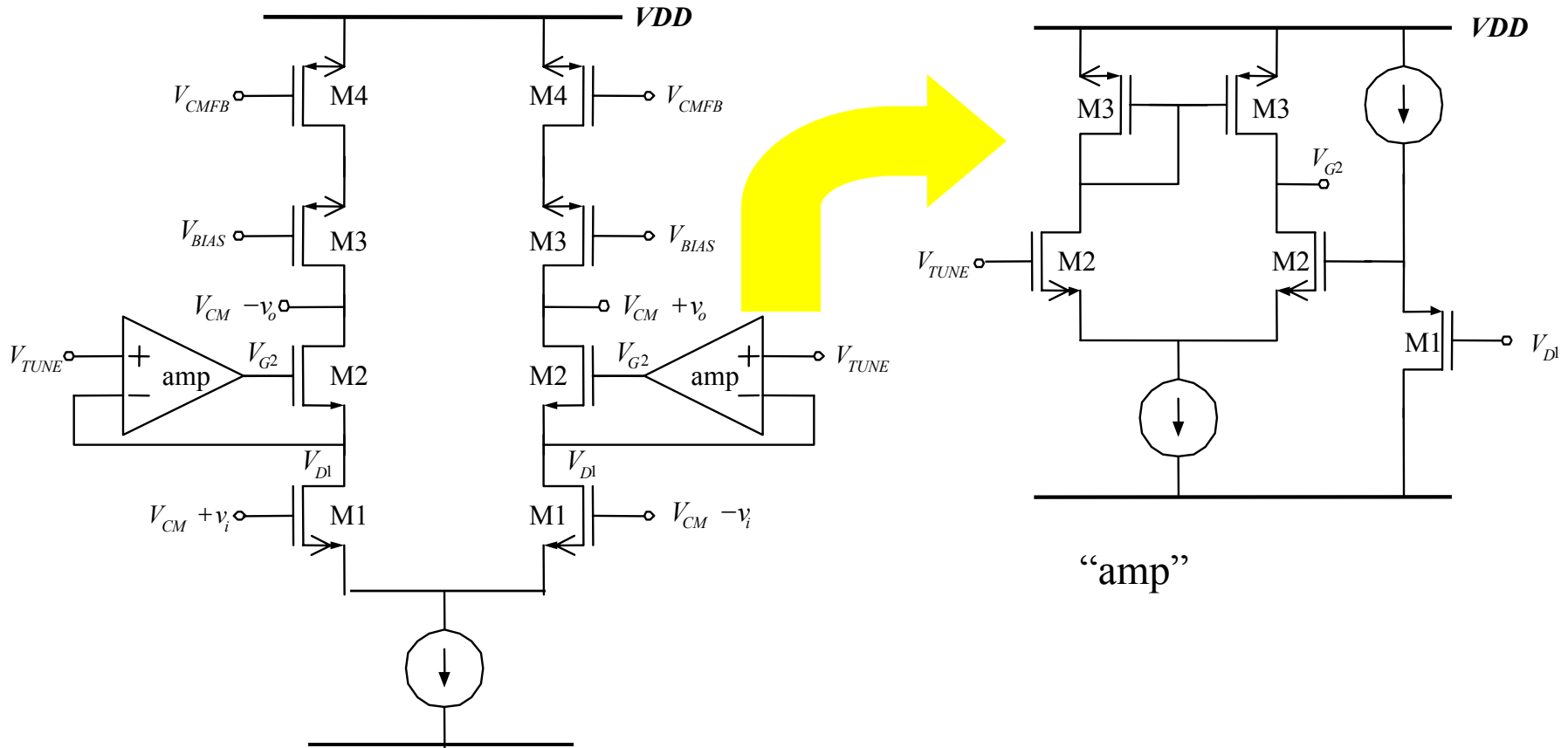


(b) Balanced OTA



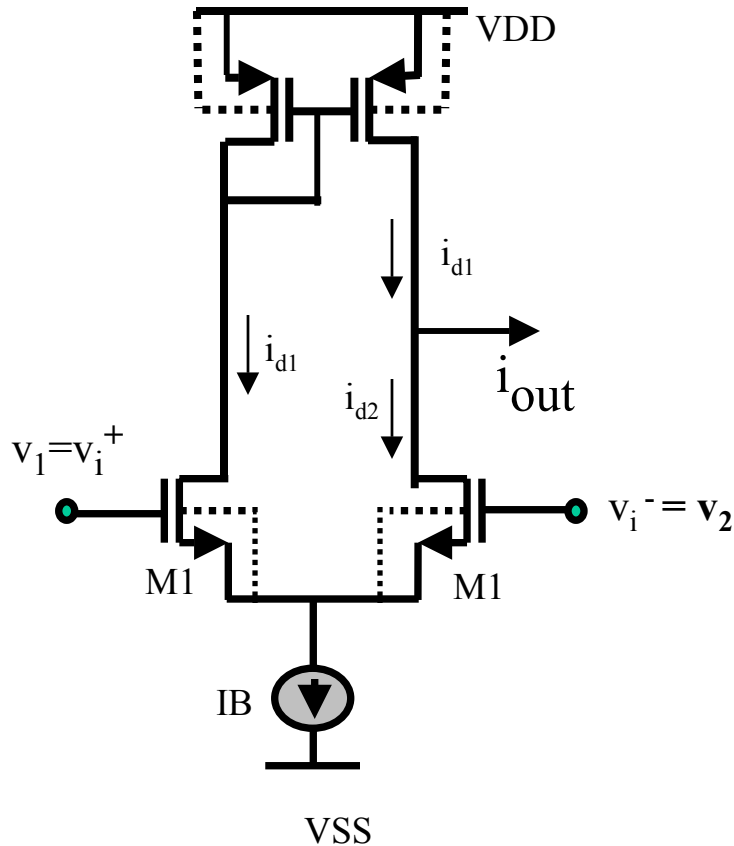
(c) Cascode

# High DC Gain Differential OTA



- Transistors M1 operate in Linear region: Wide linear range; Large tuning range;
- RGC loop: Fix  $V_{DS1}$  → better linearity.

# Basic Operational Transconductance Amplifier Characteristics



DESIGN CONSIDERATIONS:

$$\Leftrightarrow v_d = v_1 - v_2 < V_{DSAT}$$

$$\Leftrightarrow V_{1,2} - V_{SS} > V_{GS1} + V_{DSATB}$$

$$i_{out} = \sqrt{\mu_n C_{OX} \frac{W}{L} I_B} (v_1 - v_2)$$

or

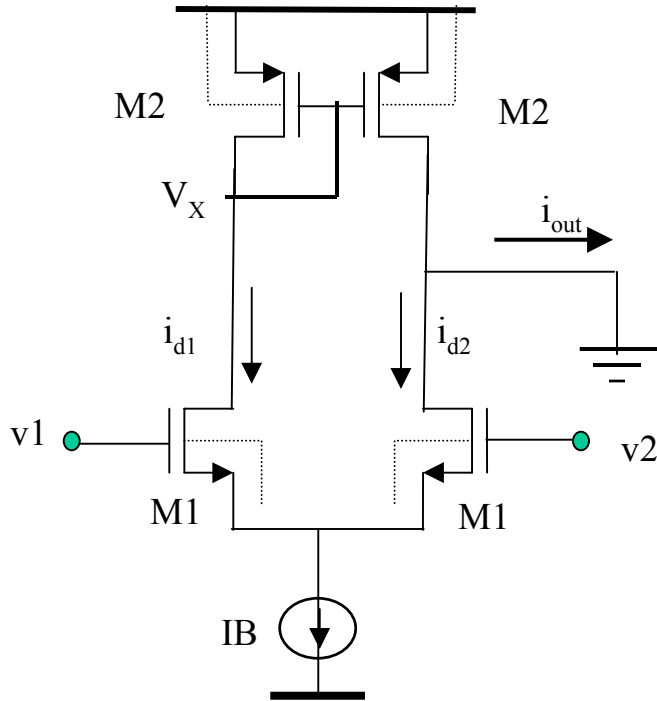
$$i_{out} = g_m (v_1 - v_2) \quad \text{Sensitive to differential signals}$$

$$v_{out} = g_m r_{out} (v_1 - v_2)$$

$$r_{out} = (g_{o1} + g_{op})^{-1}$$

$i_{out} = 0$  for  $v_1 = v_2 \Rightarrow$  rejection to common-mode signals

# Simple OTA Design Equations



$$g_m = \mu_n C_{OX} \left( \frac{W}{L} \right) V_{DSAT}$$

$$\text{Noise} \Rightarrow g_m > g_{m,\min}$$

$$GBW = \frac{g_m}{C_L}$$

$$\omega_p = \frac{g_{mp}}{C_p} \cong \mu_p \frac{V_{DSAT}}{2L_p^2}$$

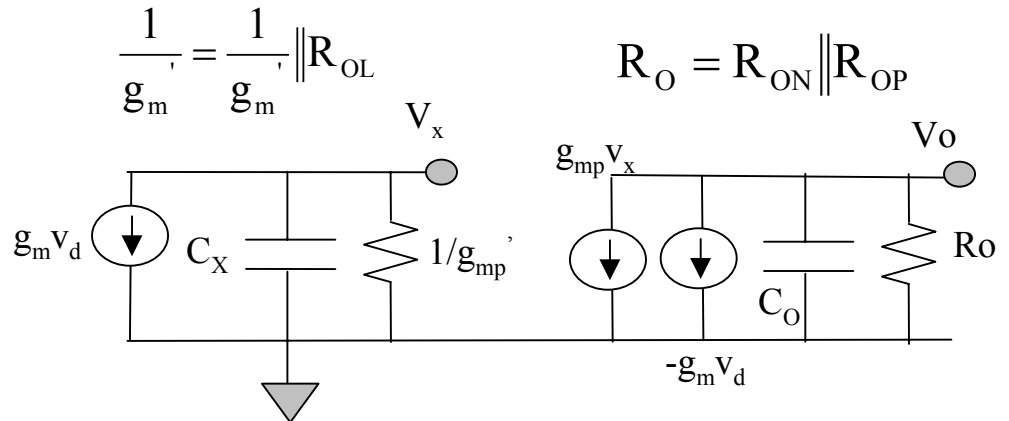
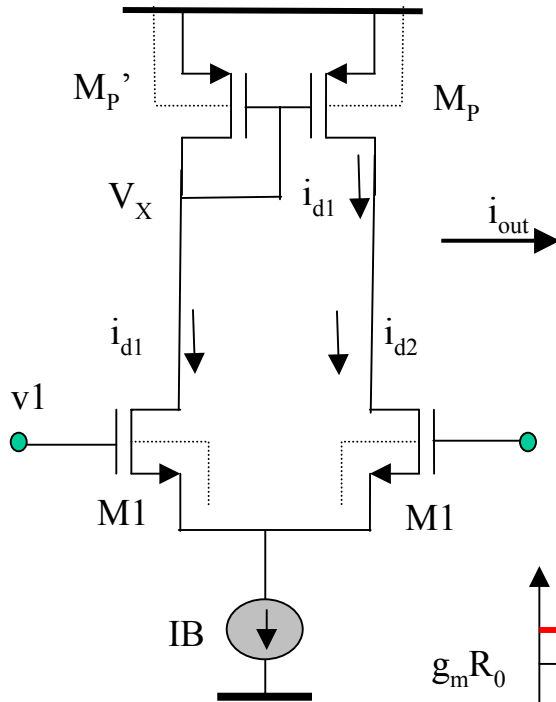
$$R_{out} \cong r_p \parallel r_n$$

$V_{DSAT}$  is limited!!

$$\text{Noise}(V_{RMS}) = \sqrt{\frac{16kT}{3}} \sqrt{\frac{1}{g_{m1}}} \sqrt{1 + \frac{g_{m2}}{g_{m1}}} (\sqrt{BW})$$

$$R_{out} \cong \frac{V_{early} L_p}{I_D}, \quad \omega_p \cong \frac{g_{mp}}{2C_{GSP}} \cong \frac{\mu_p V_{DSAT} P}{2L_p^2}$$

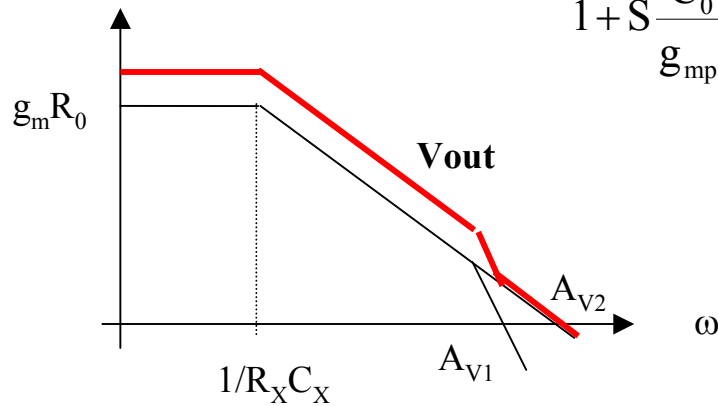
# Simple OTA Frequency Response



$$R_O = R_{ON} \parallel R_{OP}$$

$$\frac{1}{g_m'} = \frac{1}{g_m} \parallel R_{OL}$$

$$V_o = -\frac{g_m \left( \frac{g_{mp}'}{g_{mp}} \right)}{1 + S \frac{C_o}{g_m'}} \frac{R_o}{1 + S R_o C_o} V_d - \frac{g_m R_o}{1 + S R_o C_o} V_d$$



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# VERY LOW FREQUENCY FILTERS

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The Design of Analog Circuits **below 100 Hz**

is not trivial

- **$RC > 0.001$  sec**
  - if  $C = 10$  pF then  $R > 100$  MOHMS
  - for a 1 Hz filter (pace makers and other applications)
  - $C = 10$  pF,  $R = 628$  GOHMS ( $G_m = 2$  pA/V)
  - $C = 1000$  pF,  $R = 6.28$  GOHMS ( $G_m = 2$  nA/V)



## WE NEED SMALL $G_M$

For the basic OTA-C integrator,

$$\tau = \frac{C_L}{g_m} \Leftrightarrow f = \frac{g_m}{2\pi C_L}$$

- We need very small  $g_m$  for very low frequency applications
- As an example, for  $\tau = 1\text{s}$  and  $g_m = 16\text{nA/V}$ ,  $C_L = 1.6\text{ nF} !!$
- For a POLY-I POLY-II Capacitor (  $C/A \sim 600\text{ aF}/\mu\text{m}^2$  ) in the AMI  $1.2\mu$  process, this means a Si area of  $2.7\text{ mm}^2 !! \Rightarrow$  Impractical for IC's ( Tiny chip area  $\sim 4\text{ mm}^2$  )

# How can we tackle this low frequency ( large time constant ) design problem ?

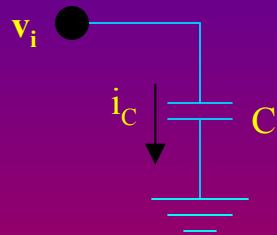
Possible Solutions for high-performance Very small transconductance

OTA's circuits involve operating transistor in their transistion region and:

- Current division techniques
- Floating Gate Techmiques
- Bulk- Driven transistors
- Impedance scalers
  - $Z \implies NZ$  or  $Z/N$  ( $C \implies NC$ )
  - low-noise impedance scalers
  - small silicon area

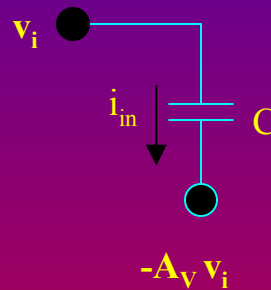
# IMPEDANCE SCALERS

Single capacitor



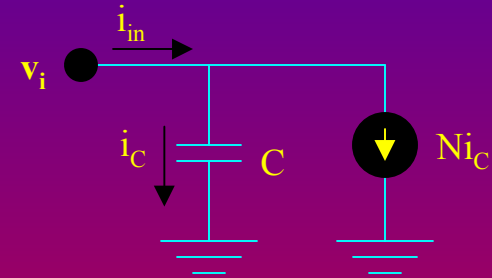
$$i_C = (sC)v_i$$

Voltage amplifier



$$i_{in} = (sC(1 + A_V))v_i$$

Current amplifier



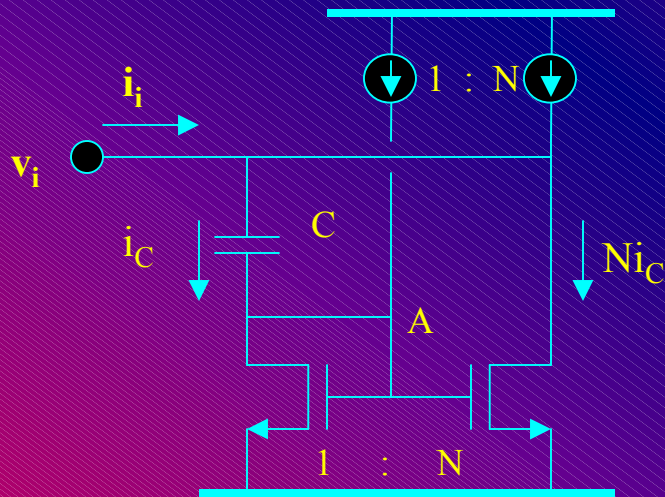
$$i_{in} = (sC(1 + N))v_i$$

Remarks:

⇒ Voltage amplification is useless for low-voltage continuous-time filters.

⇒ Impedance scaler based on current amplification is precise for moderated  $N$ .

# CAPACITOR MULTIPLIER CIRCUIT IMPLEMENTATION



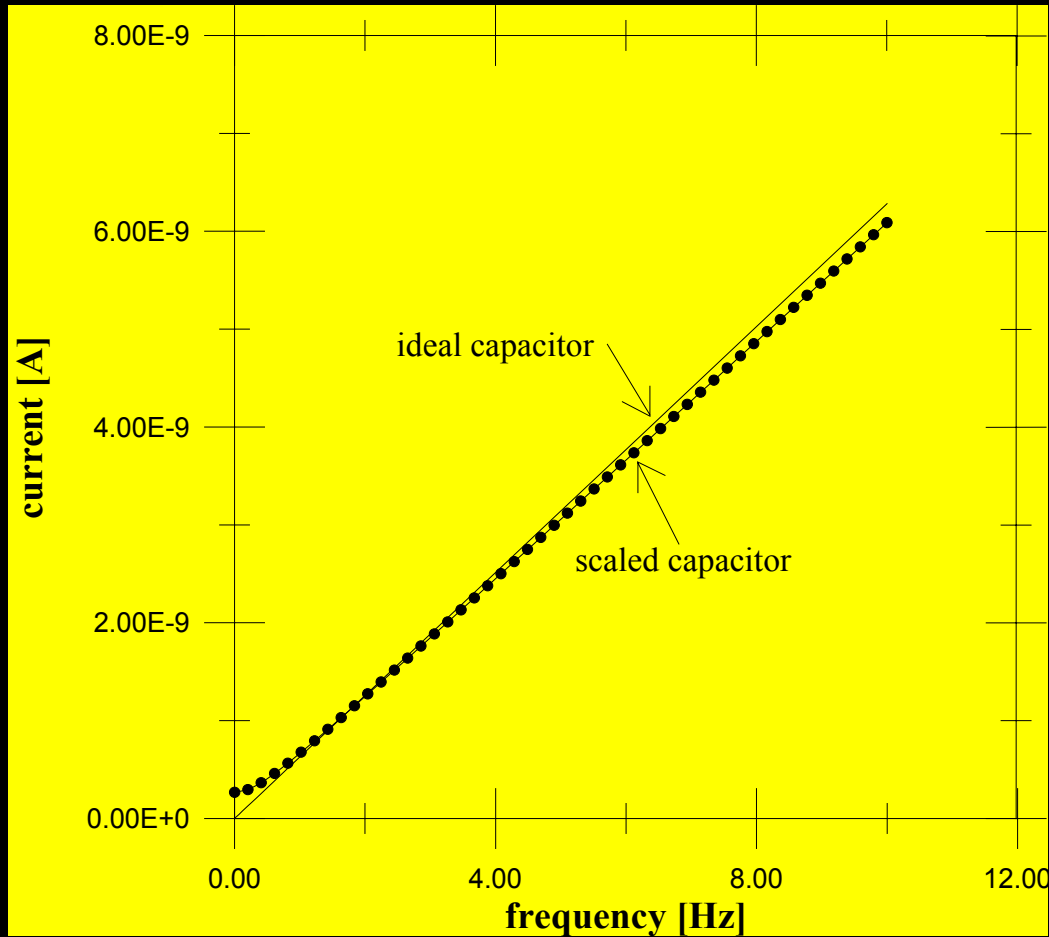
$$\frac{v_i}{i_i} = \frac{v_i}{(N+1)i_c}$$

$$Z_{eq} = \frac{1}{s[(N+1)C]}$$

The following conditions must be satisfied:

- ➔ Low impedance at node A
- ➔ Transistor output resistance can be neglected
- ➔ Current gain is precise

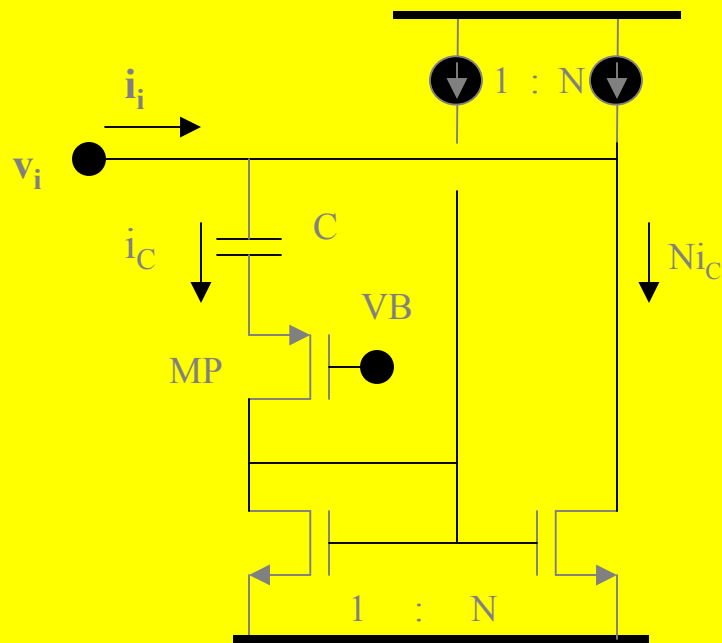
# DESIGN EXAMPLE: Capacitor Multiplier



100 pF capacitor.

Scaled capacitor uses a 5 pF capacitor and  $N=19$ .

# IMPROVING ITS FREQUENCY RESPONSE



Cascode transistor improves frequency response

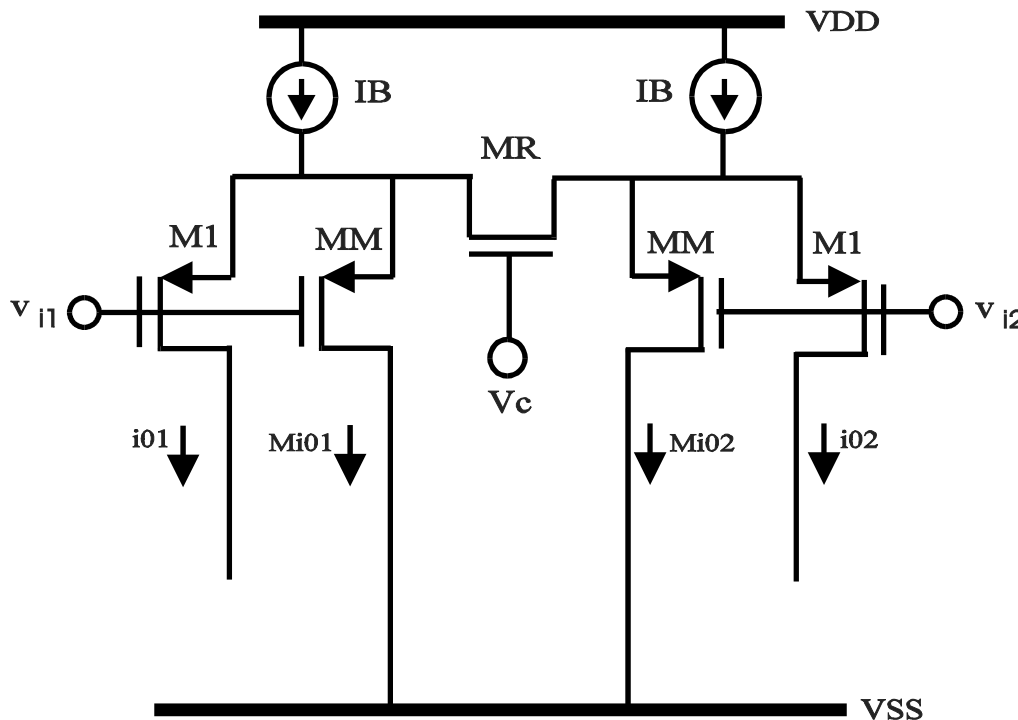
Design procedure:

MP is optimized for frequency.

N-type transistors are optimized for precision.

The loop must be stable

# CURRENT DIVISION PRINCIPLE PLUS SOURCE DEGENERATION TRANSCONDUCTANCE



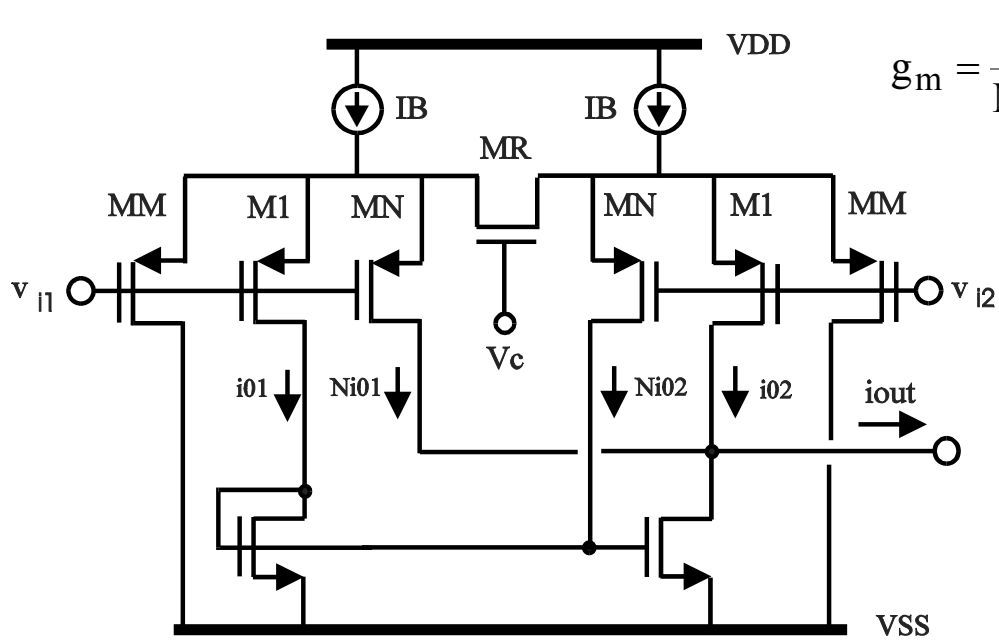
$$HD \propto \frac{v_{i1} - v_{i2}}{V_{GS} - V_T}$$

$$\frac{i_{01} - i_{02}}{v_{i1} - v_{i2}} = \frac{2\mu C_{OX}}{M+1} \frac{W_R}{L_R} (V_{GS} - V_T)$$

$$M = \frac{g_{mm}}{g_{m1}}$$



# OTA FOR VERY LOW-FREQUENCY APPLICATIONS

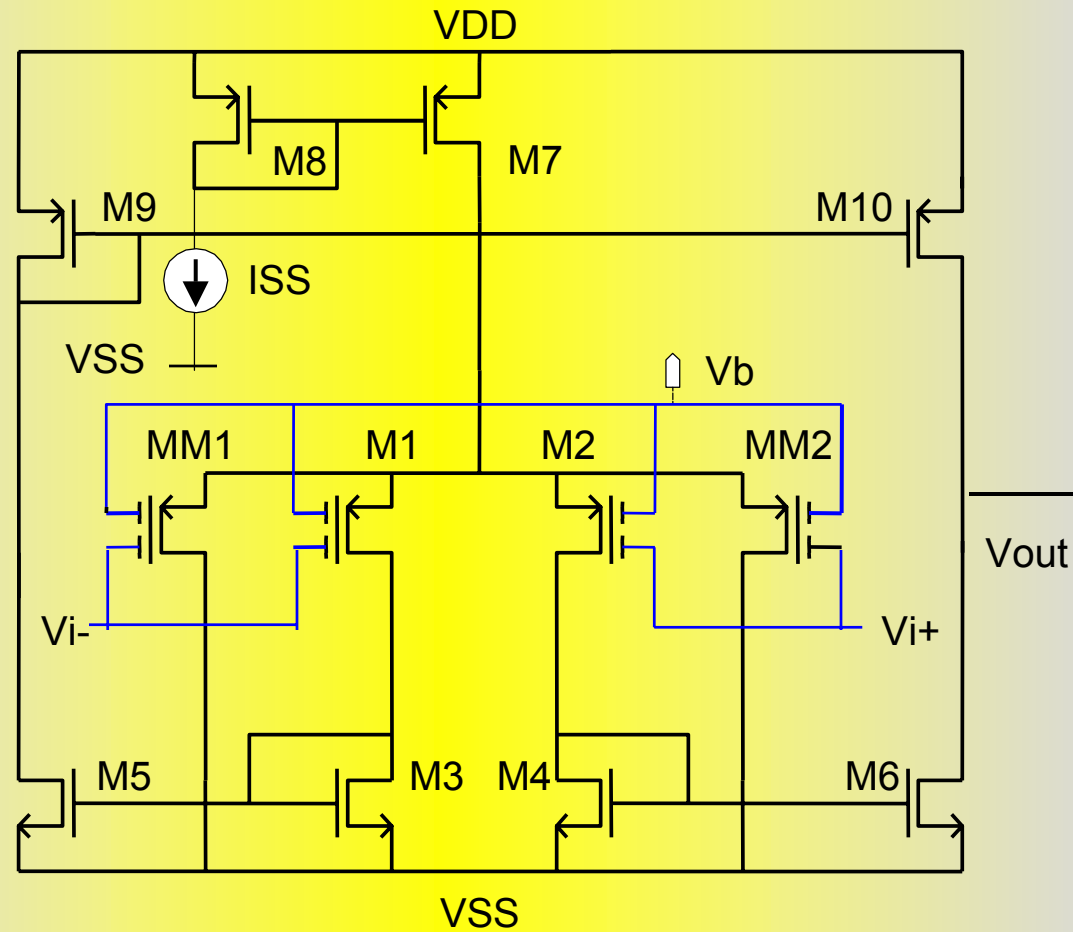


$$g_m = \frac{2(N-1)}{M+N+1} \left( \mu C_{OX} \frac{W_R}{L_R} (V_{GS} - V_T) \right)$$

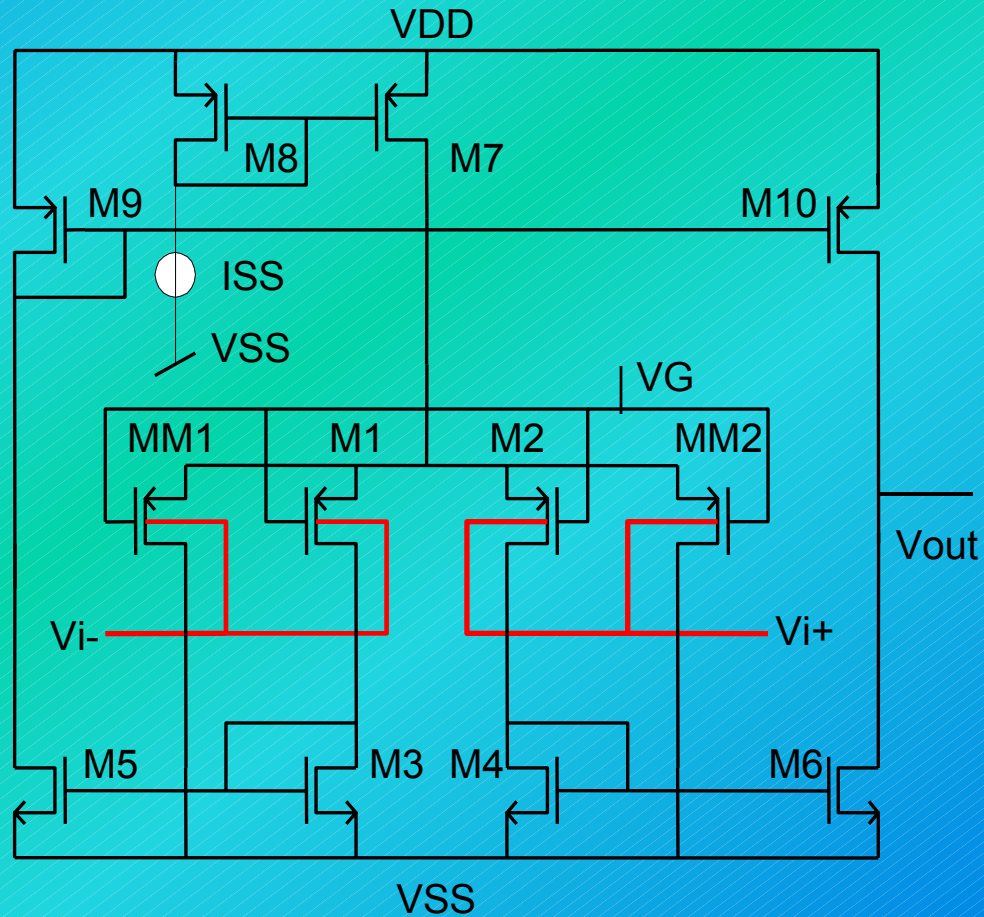
$$M = \frac{\left( \frac{W}{L} \right)_{MM}}{\left( \frac{W}{L} \right)_{M1}}$$

$$N = \frac{\left( \frac{W}{L} \right)_{MN}}{\left( \frac{W}{L} \right)_{M1}}$$

# Floating Gate plus Current Division OTA

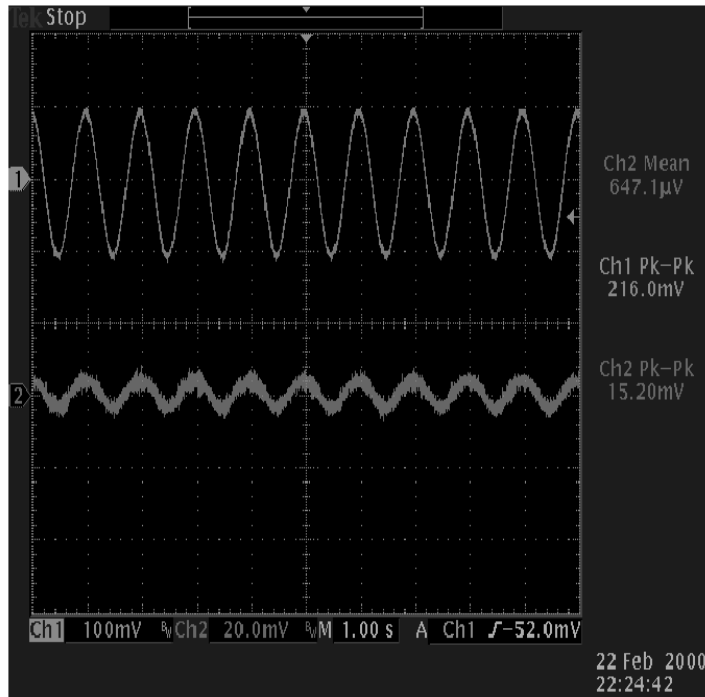


# Bulk Driven plus Current Deviation OTA

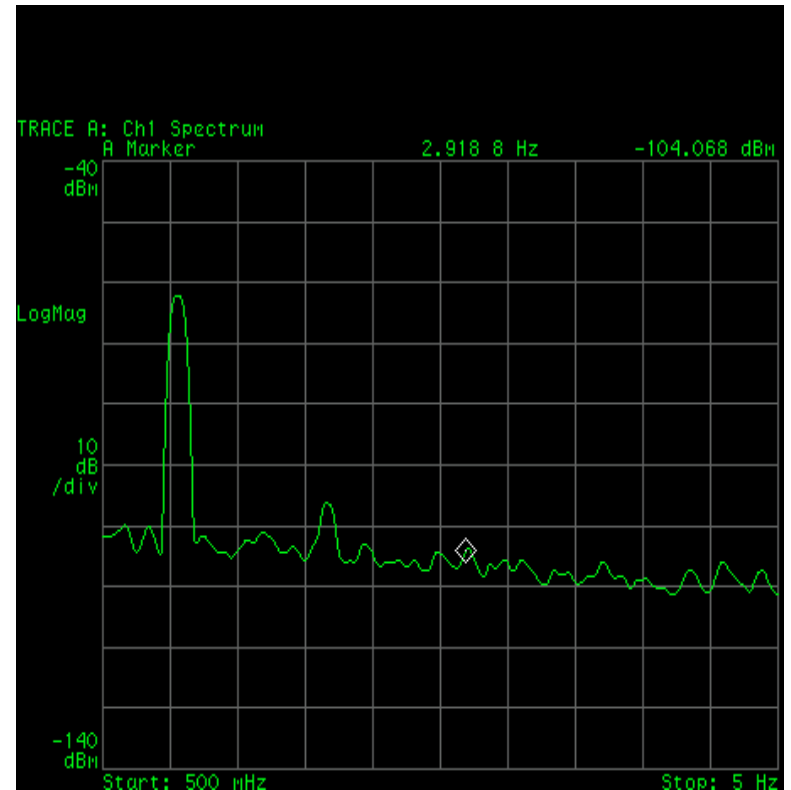


# BULK DRIVEN OTA

## EXPERIMENTAL RESULTS (0.5 $\mu\text{m}$ )



Input Ch1 214mVpp @ 1 Hz  
Output Ch2 15.2mVpp



THD  $\sim$  -39dBm  $\sim$  1.1% @214mVpp, 1Hz

## EXPERIMENTAL RESULTS FOR THE DIFFERENT OTA DESIGNS

PARAMETER	REFERENCE	SD+CD	FG+CD	BD+CD
$G_M$ (nA/V)	9.4	9.3	9.2	9.4
HD <sub>3</sub> (%)	0.9@162mV <sub>pp</sub>	1.0@242mV <sub>pp</sub>	1.1@330mV <sub>pp</sub>	0.9@900mV <sub>pp</sub>
Input noise ( $\mu$ V <sub>rms</sub> )	18.1	26.1	39.1	104.7
SNR@1%HD <sub>3</sub> (dB)	69.9	70.3	69.5	69.6
I <sub>BIAS</sub> (nA)	2.6	120	232	560

Key:

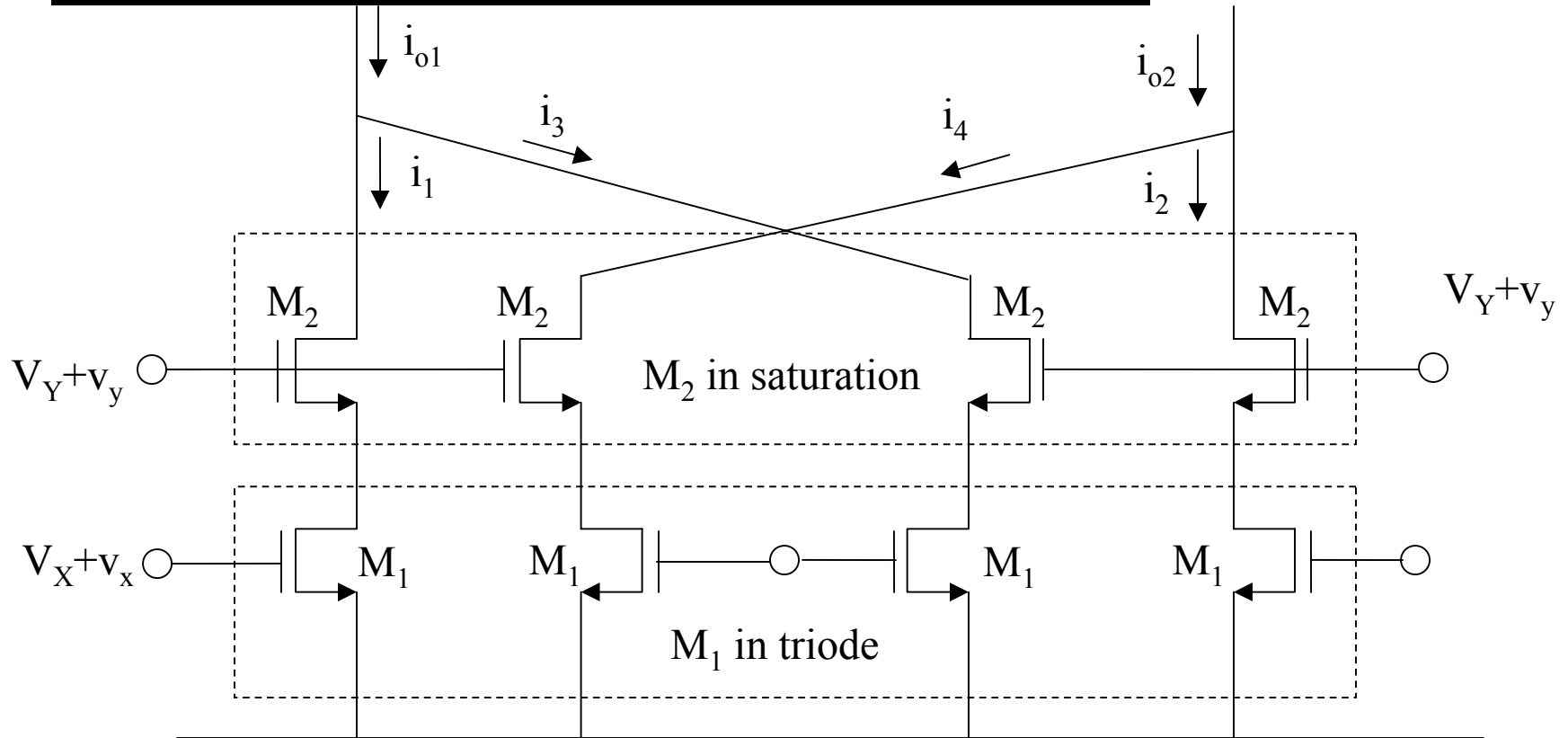
SD source degeneration

CD current division

FG floating gate

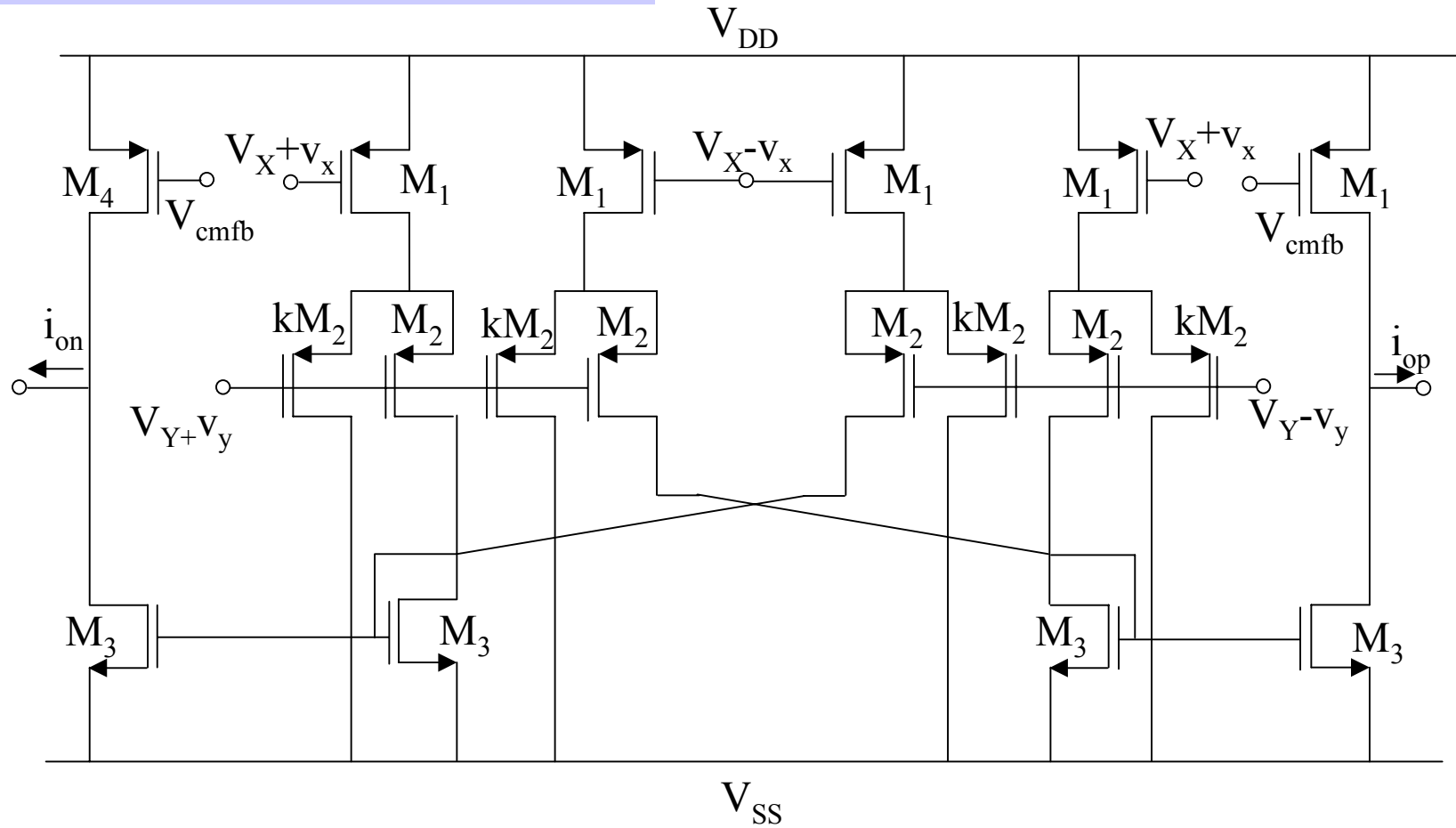
BD bulk driven

# How to make a transconductor with a wide Gm tuning range?



Basic topology of the four-quadrant multiplier

# Multiplier-based OTA with CD



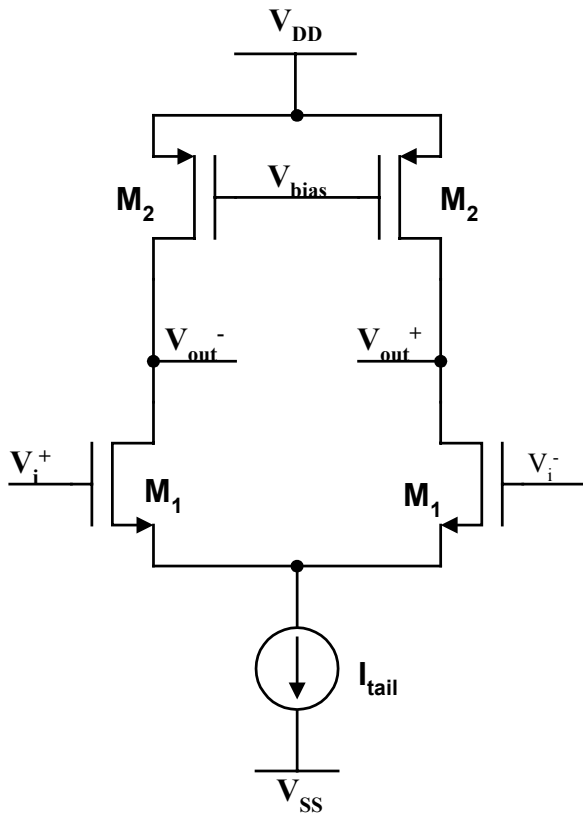
$$G_{Md}(v_x) \equiv \frac{i_{od}}{2v_y} = \left[ \left( \frac{4\mu C_{ox}W}{L} \right)_{M_1} \left( \frac{1}{k+1} \right) \right] v_x$$

# **Fully Differential and Pseudo Differential OTAs**

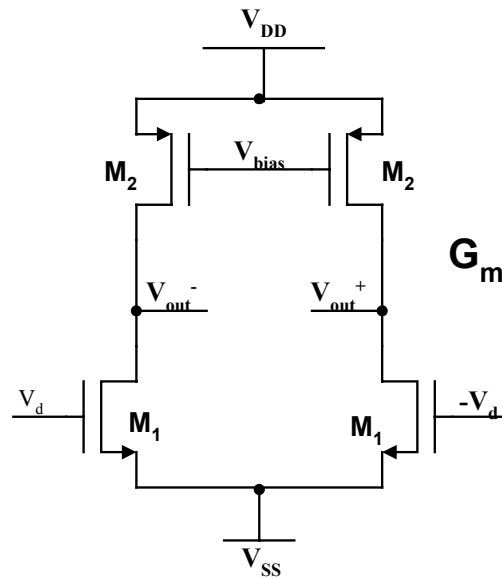
Common - Mode Feedforward and  
Feedback strategies needed for  
differential output filters

# Fully Differential OTA Characteristics

Simple Differential OTA  
With tail Current Source

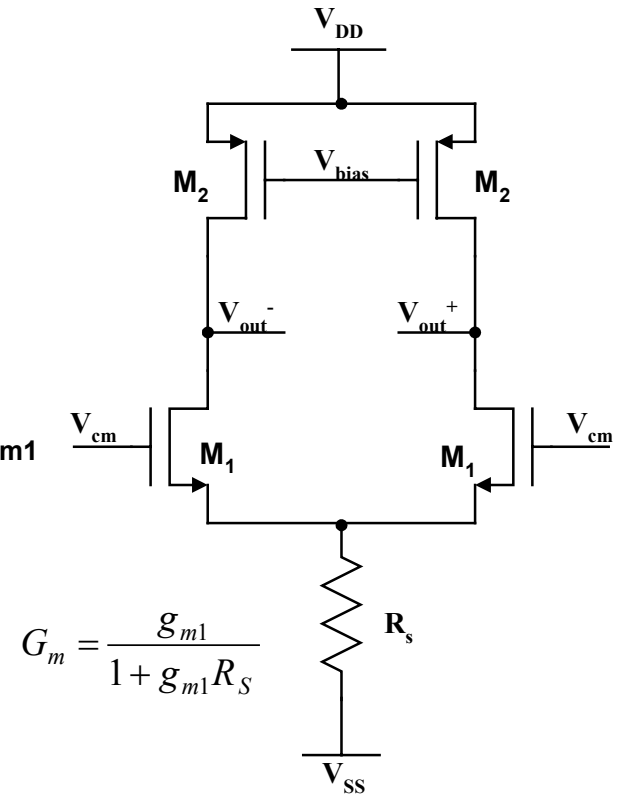


Differential-Mode



$$G_m = g_{m1}$$

Common-Mode

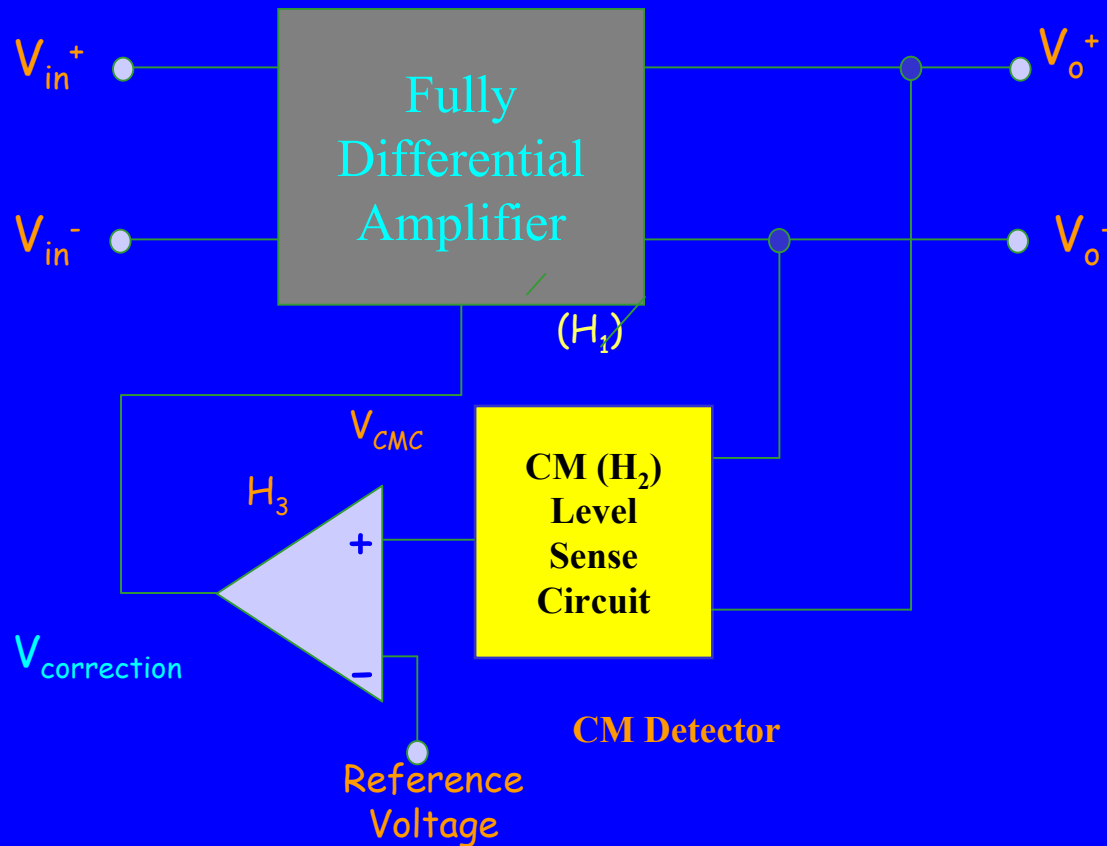


$$G_m = \frac{g_{m1}}{1 + g_{m1}R_s}$$

- ✗ Limited linear input range
- ✗ Limited tuning range

- ✓ Reasonable Common-mode gain
- ✓ Reasonable PSRR

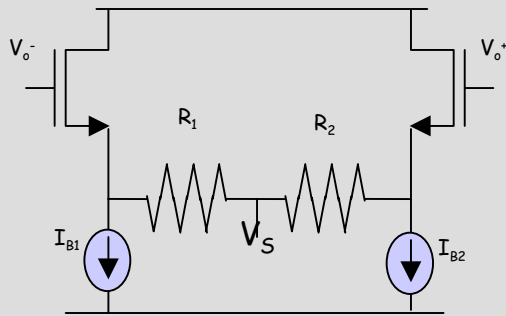
# Conceptual Architecture of Common-Mode Feedback Loop



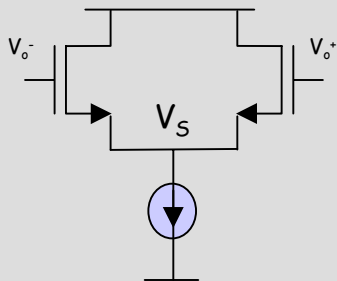
# CM signal detectors : two conventional cases

$$V_S = \alpha_1 v_{o,cm} + \alpha_2 v_{o,dm} + \alpha_3 v_{o,dm}^2$$

## CM Detector



## CM Detector



## Performance

$$\alpha_1 = 1$$

$$\alpha_2 = \frac{\Delta R}{4R} + \frac{1}{\sqrt{8\beta I_B}} \cdot \frac{\frac{\Delta R}{2R} + \frac{\Delta I_B}{4I_B} + \frac{\Delta\beta}{4\beta}}{2R + \sqrt{\frac{2}{\beta I_B}}}$$

$$+ \frac{1}{\sqrt{8\beta I_B}} \cdot \frac{\Delta V_T + \frac{\Delta I_B}{2I_B} \sqrt{\frac{2I_B}{\beta}}}{I_B \left( 2R + \sqrt{\frac{2}{\beta I_B}} \right)^2}$$

$$\alpha_3 = \frac{1}{2I_B} \cdot \frac{1}{\sqrt{8\beta I_B}} \cdot \frac{1}{\left( 2R + \sqrt{\frac{2}{\beta I_B}} \right)^2}$$

$$\alpha_1 = 1$$

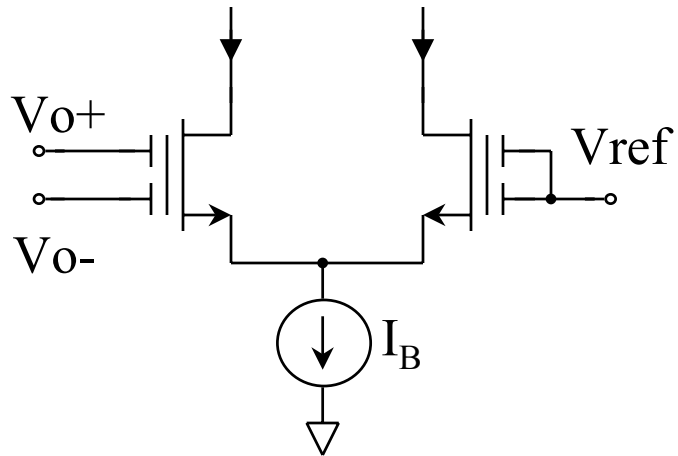
$$\alpha_2 = \frac{\Delta\beta}{4\beta} + \frac{\Delta V_T}{4} \cdot \sqrt{\frac{\beta}{I_B}}$$

$$\alpha_3 = \frac{1}{8} \sqrt{\frac{\beta}{I_B}}$$

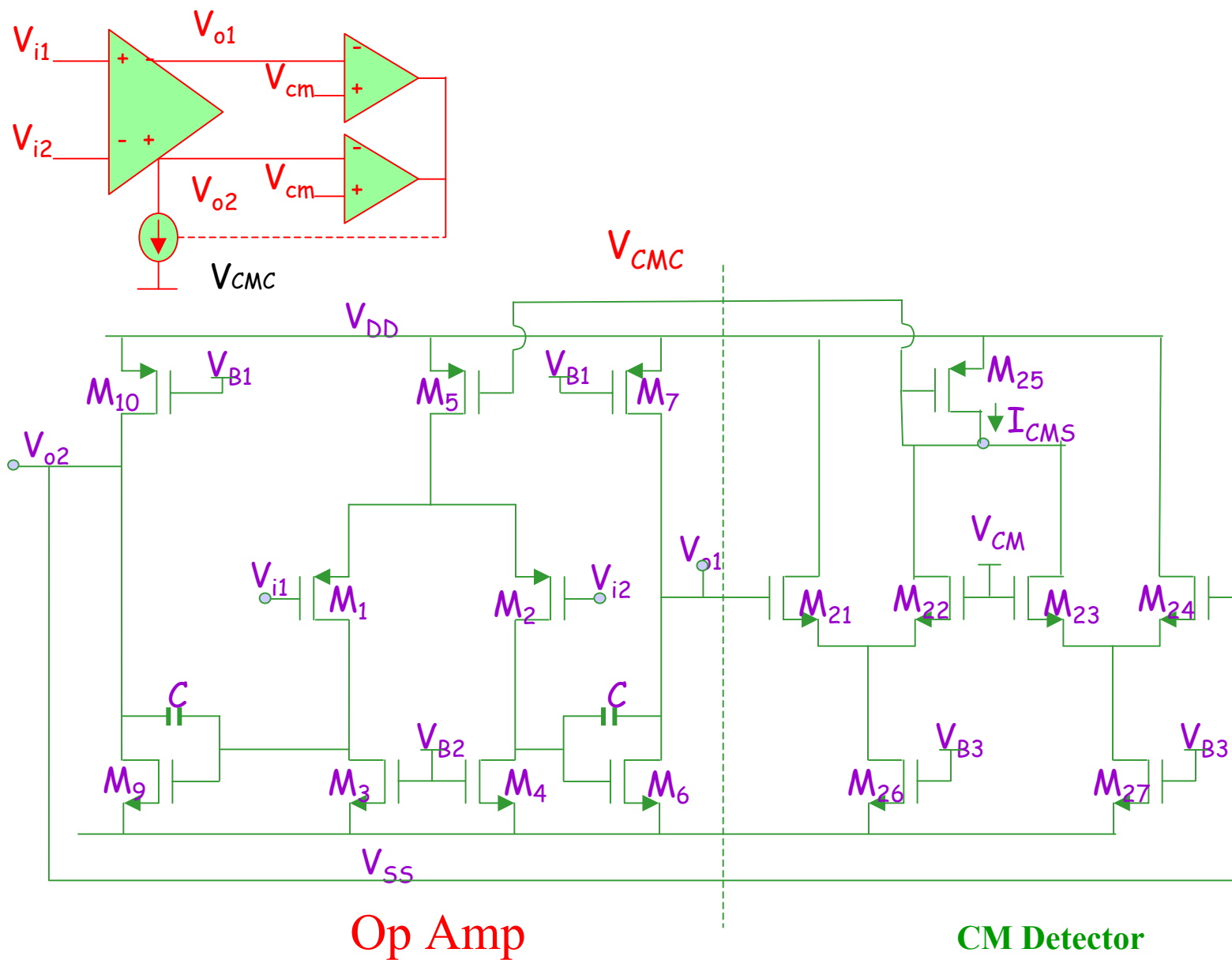
## Observations

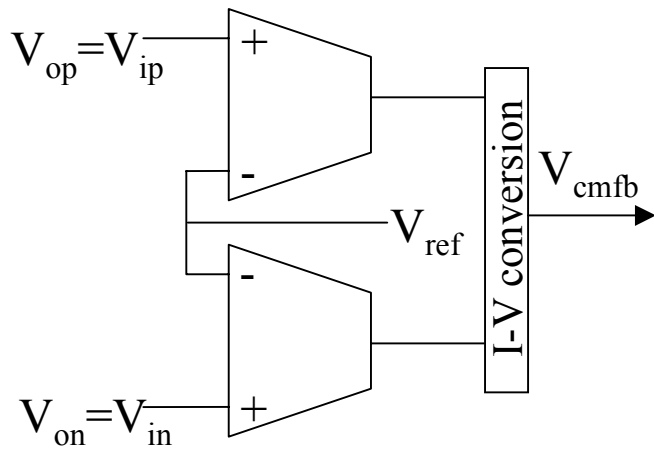
- High DC offset due to source followers
- Other buffers can be used to reduce the DC offset
- Mismatching between the passive resistors is the dominant error in  $\alpha_2$
- Highly non-linear CM signal detector

## Floating Gate Non-conventional Differential Pair for common mode detection

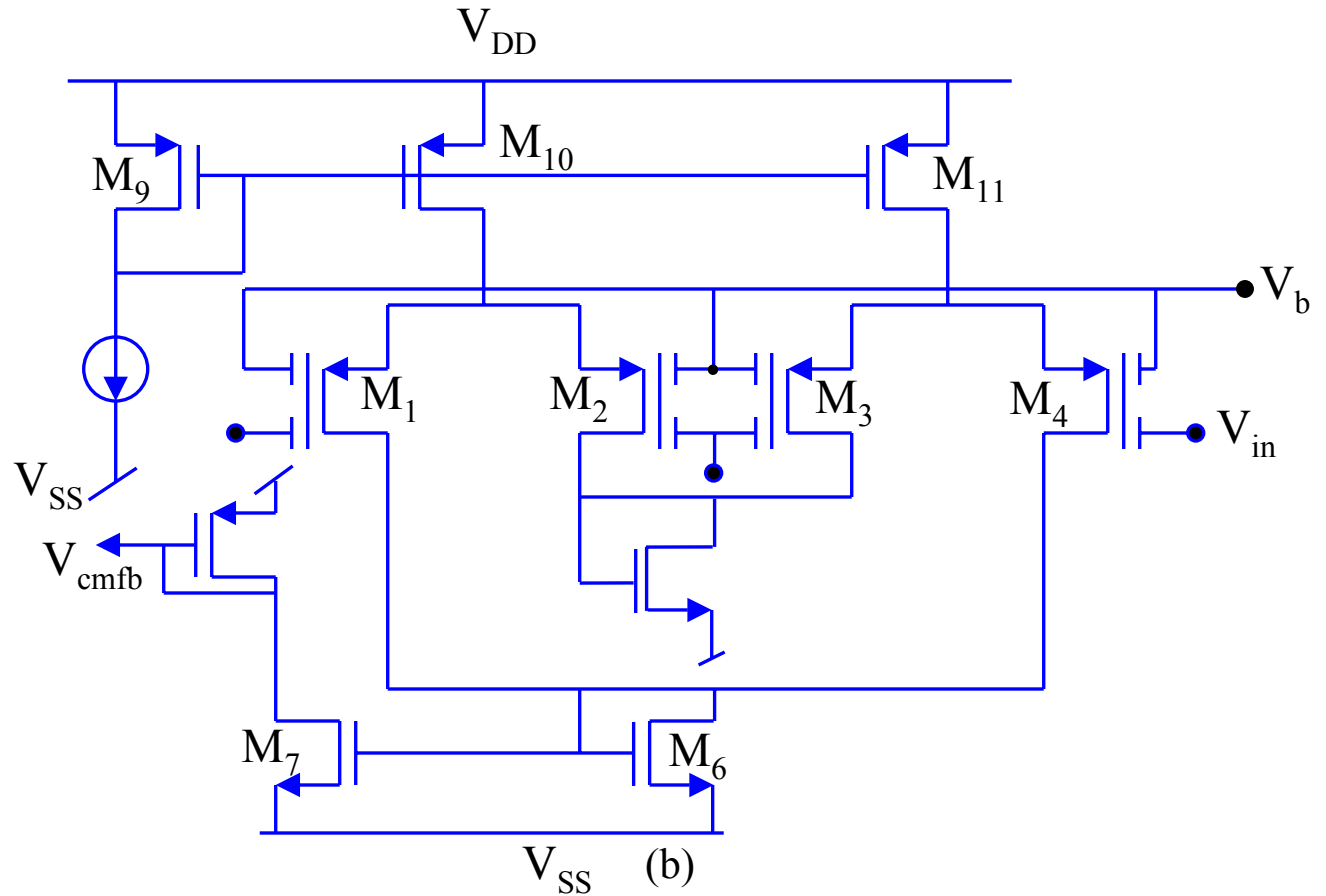


# Example of a compensated Op Amp and a CM sense circuit





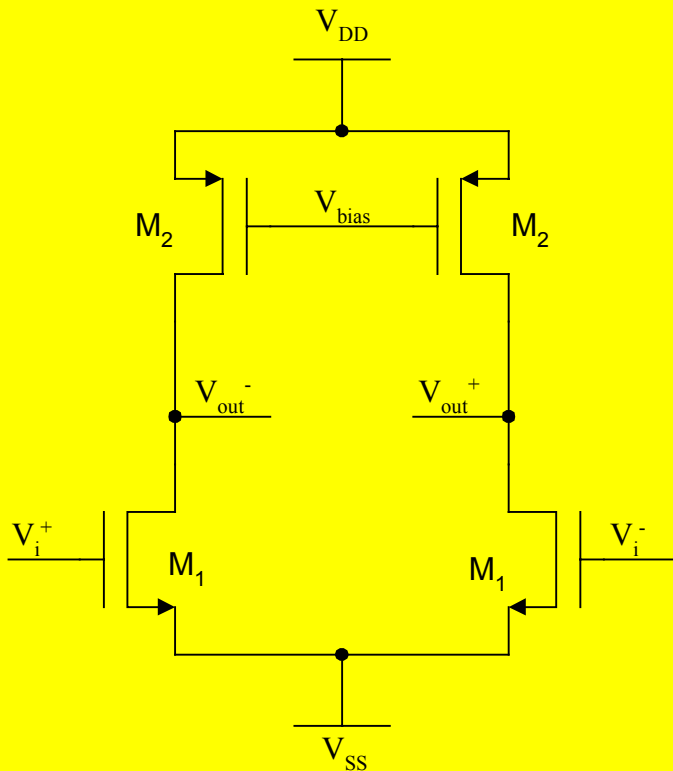
(a)



(b)

Common-mode feedback circuit. (a) Block diagram. (b) Circuit using floating gates.

# Pseudo Differential Transconductance



Simple Pseudo  
Differential OTA

## Advantages

- ✓ Suitability for low voltage
- ✓ Wider common-mode input range

## Disadvantages

- ✗ Poor common-mode gain

$$A_{CM} = A_{DM} \gg 1$$

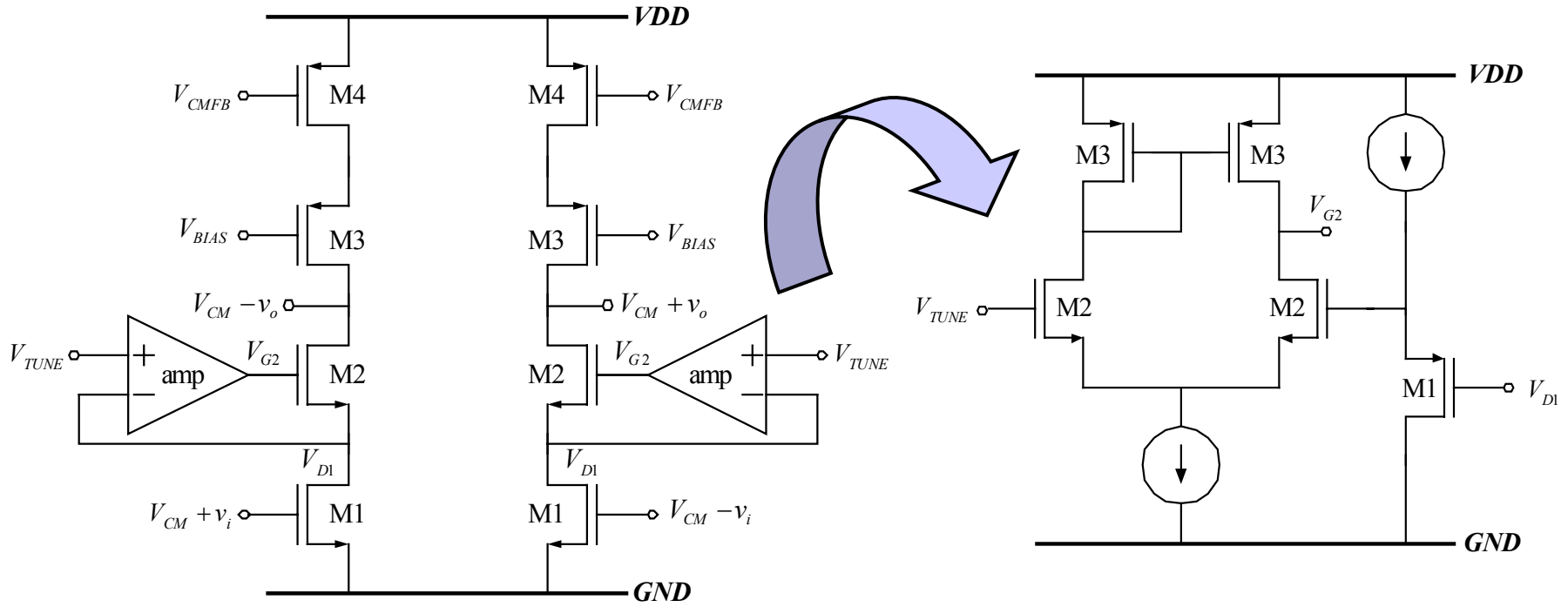
- ✗ Poor PSRR

- ✗ Low output impedance

- ✗ Need for fast and strong Extra CMFB Circuit to

- (1) Fix output common-mode voltage
- (2) Suppress common-mode signals

# Pseudo-Differential OTA with large output impedance

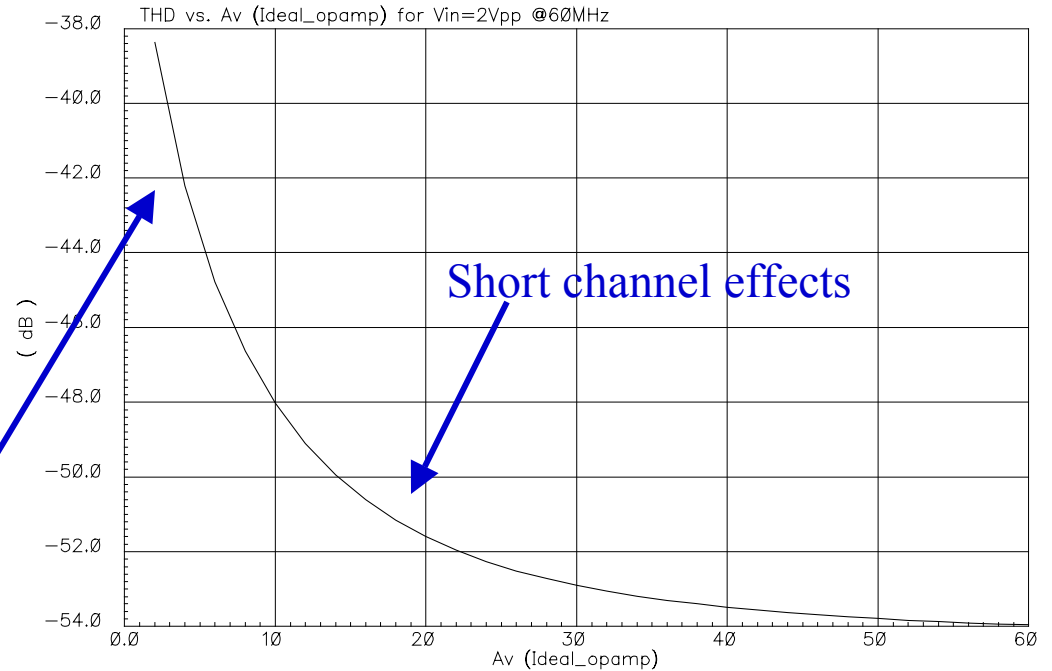
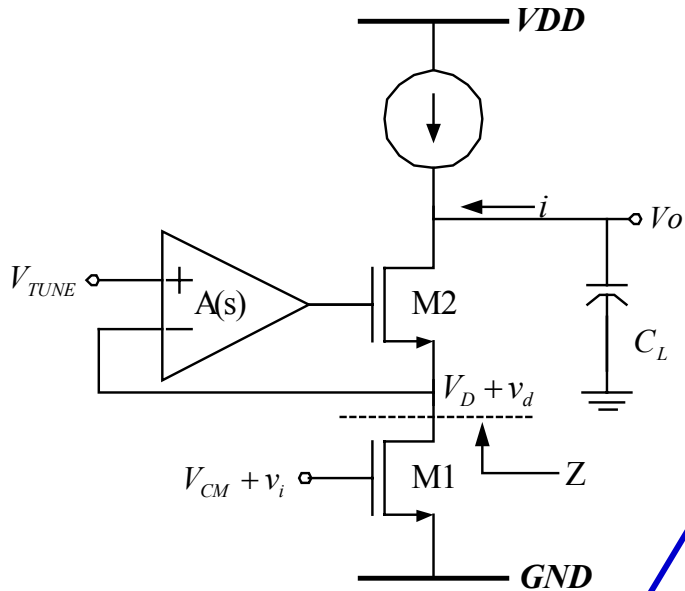


Pseudo-differential OTA

RGC amplifier “amp”

- Transistors M1 operate in Linear region: Wide linear range; Large tuning range;
- RGC loop: Fix  $V_{DS1}$  → provides better linearity.

# OTA Design Issues: RGC Loop



$$HD3 \approx \frac{V_i^2}{4} \cdot \frac{\beta^2}{[A(s)g_{m2} + \beta(V_{CM} - V_{TN} - V_D)]^2}$$

➡ OTA Gm's Linearity: Limited by how well the drain voltage of the input transistor is fixed.

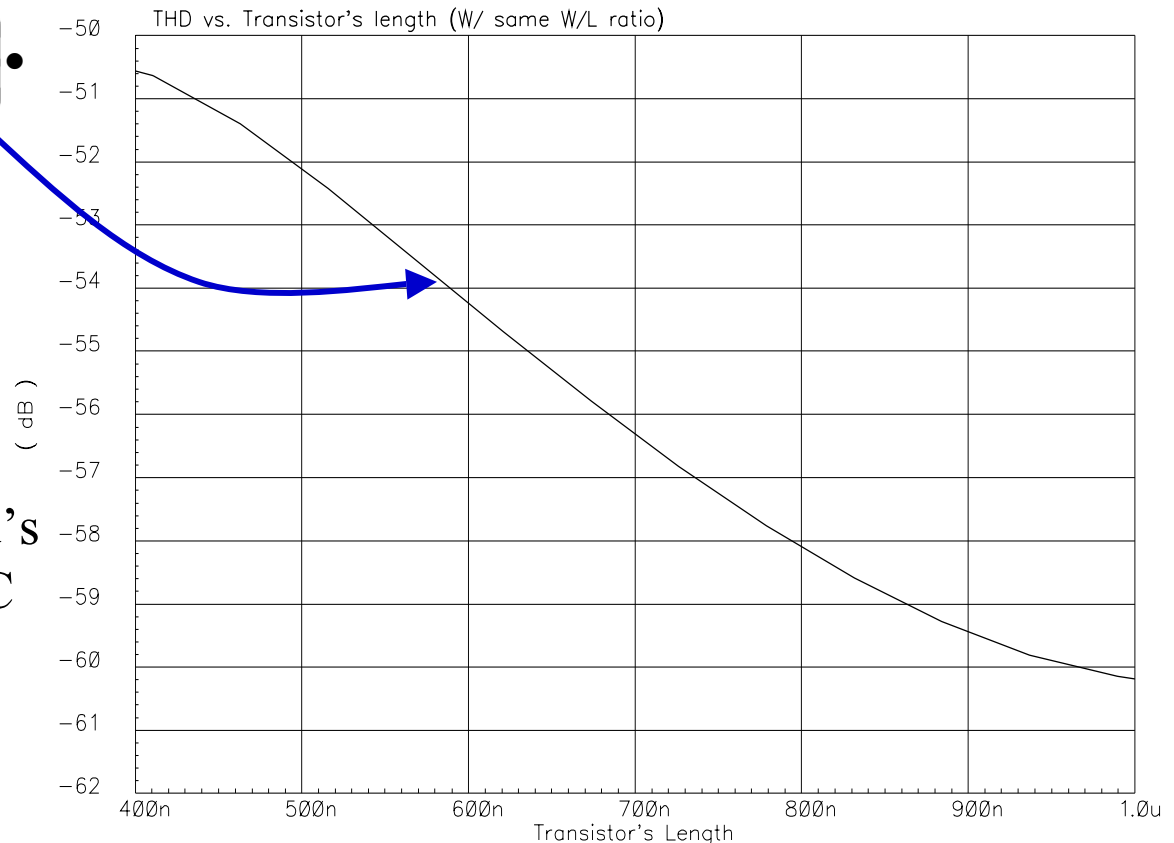
# Design Issues: Short-Channel Effects

$$\mu_{\text{eff}} = \mu_0 \left( \frac{1}{1 + \theta(V_{\text{GS}} + v_{\text{gs}} - V_{\text{T}})} \right) \cdot \left( \frac{1}{1 + \frac{1}{L\epsilon_c} \cdot (V_{\text{DS}} + v_{\text{ds}})} \right)$$

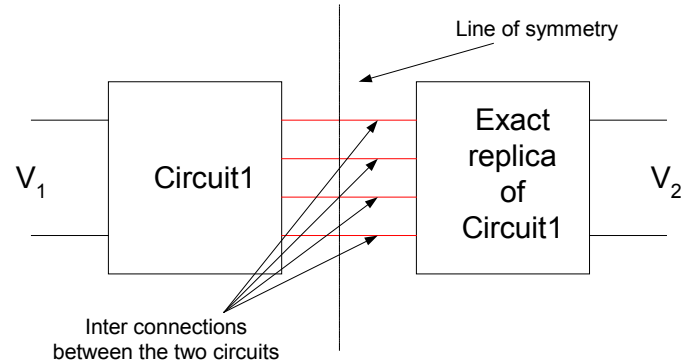
➡ Transversal electric field's effect is reduced by RGC loop;

➡ Trade-off:

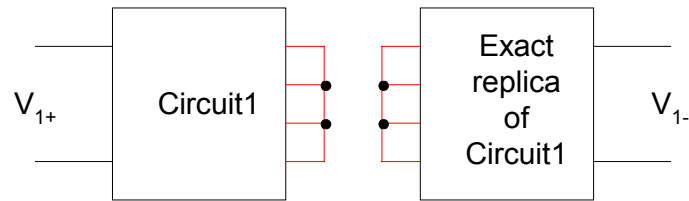
THD vs. Frequency response



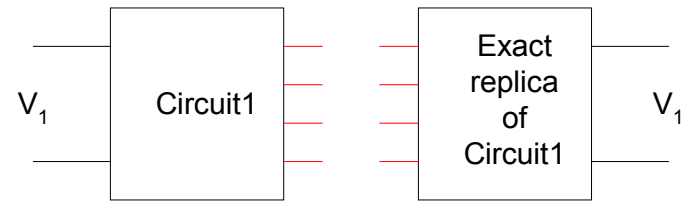
# Behavior of symmetric circuits



An example of fully symmetric circuit

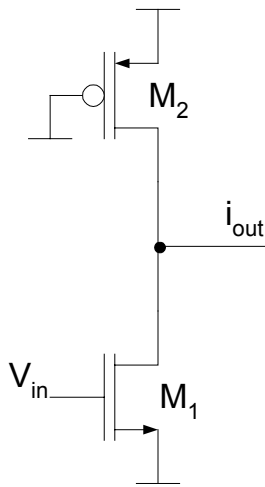


Equivalent circuit for fully differential input

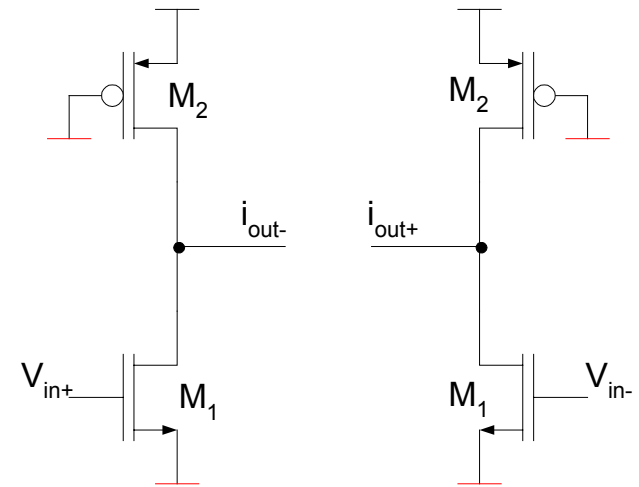


Equivalent circuit for common mode input

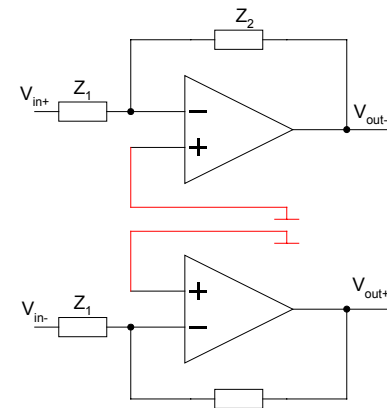
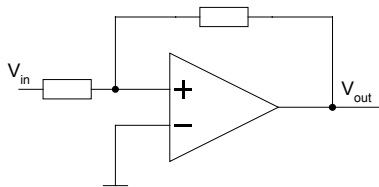
# Derivation of CMFF Pseudo-differential OTA

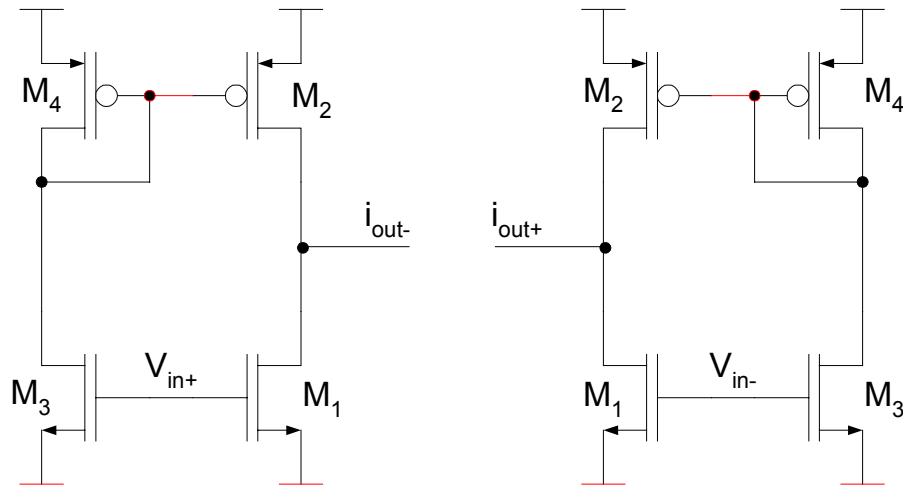


Single ended OTA circuit

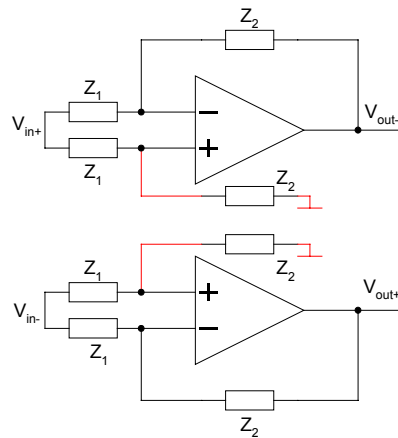


Circuit of OTA for differential input

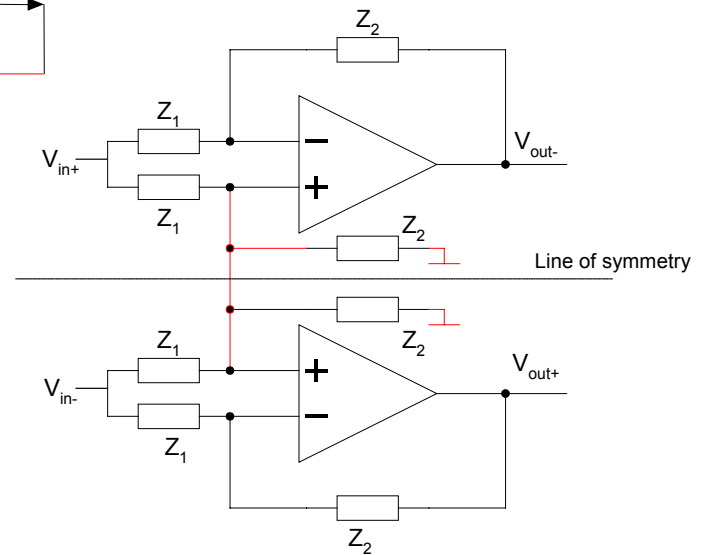
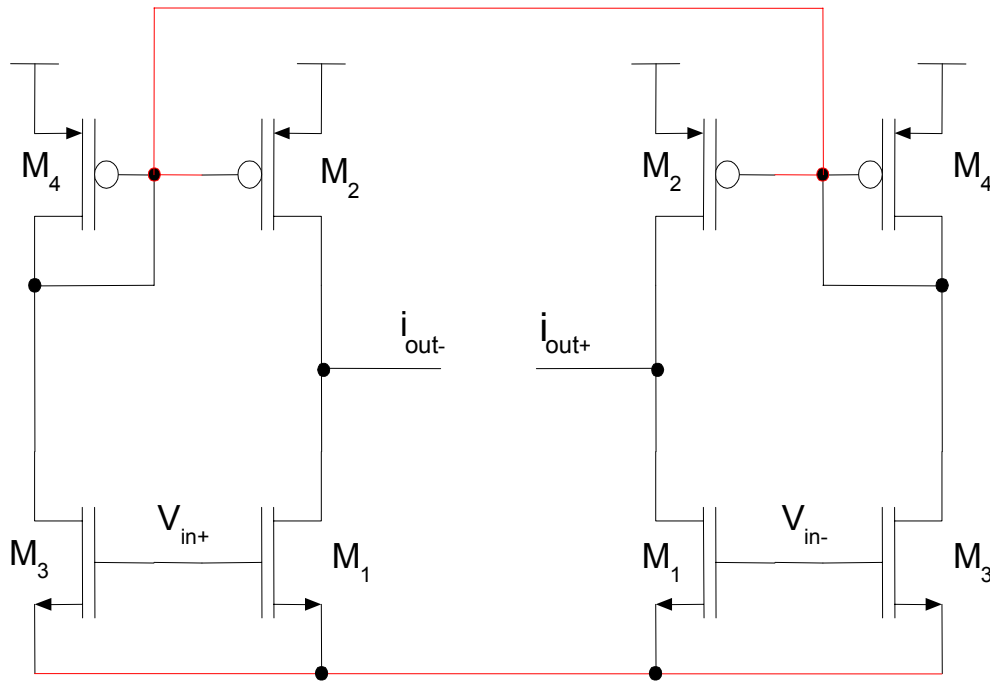




Circuit of OTA for common mode signals



# Fully-balanced, fully-symmetric **CMFF** OTA



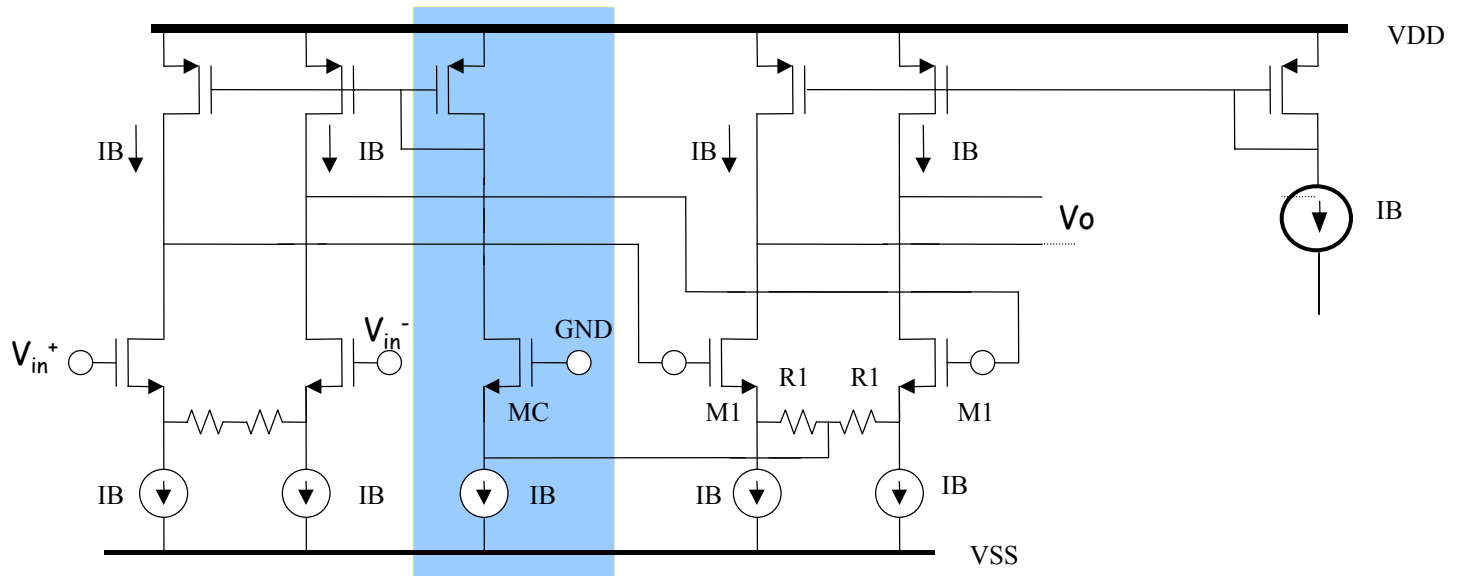
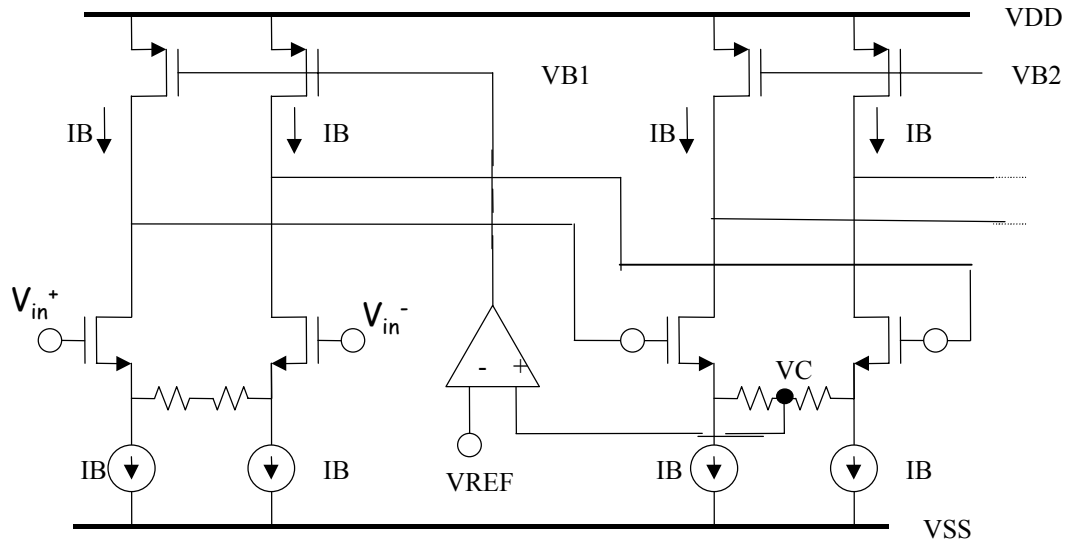


**What are the Solutions to  
Overcome those Limitations?**

# CMFB FOR OTAs: Solution 1

Typical OTA connection in pseudo-differential OTA-C based circuits.

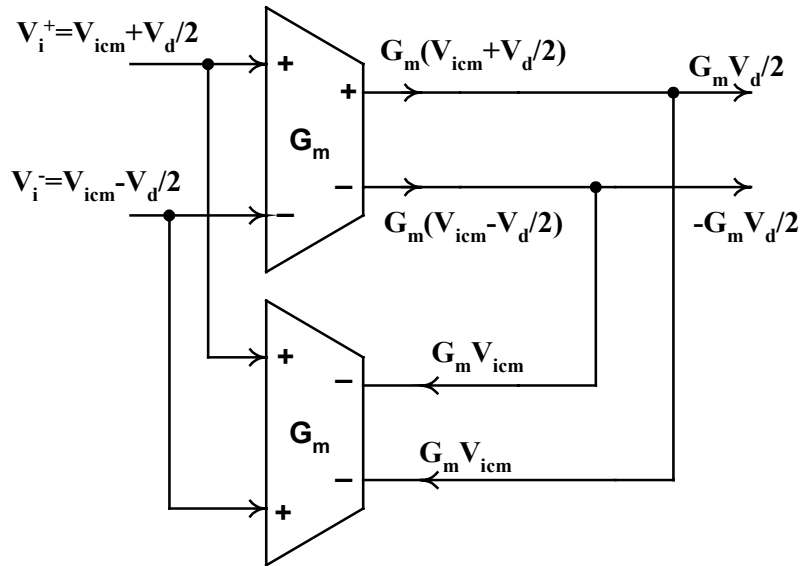
The common-mode voltage is obtained from the input of the following stage. Poor PSRR



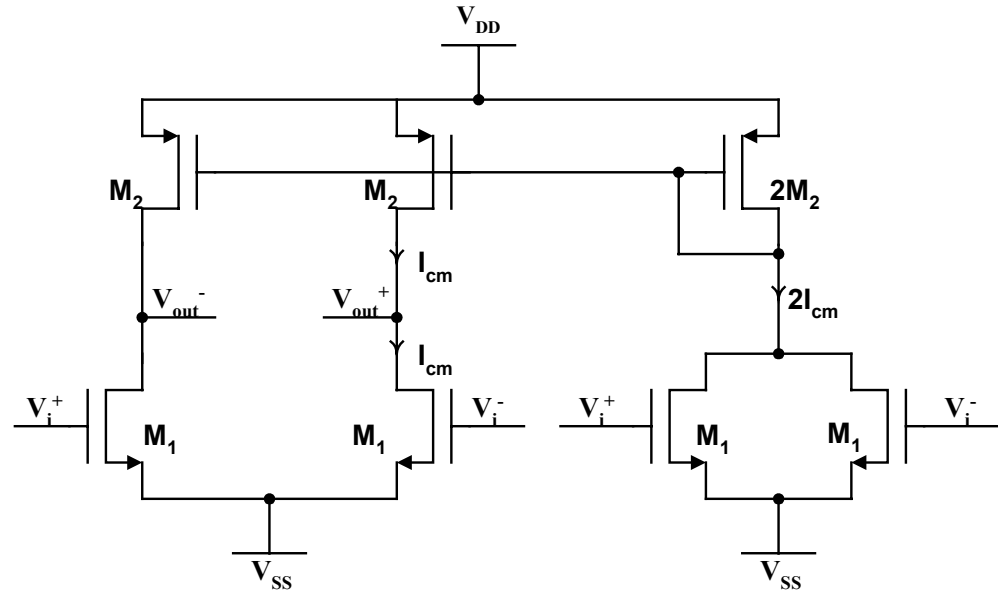
Pseudo-differential OTAs including the  
CMFB for the first one with good PSRR

# A PD Solution 2 In the Literature

Differential Mode OTA



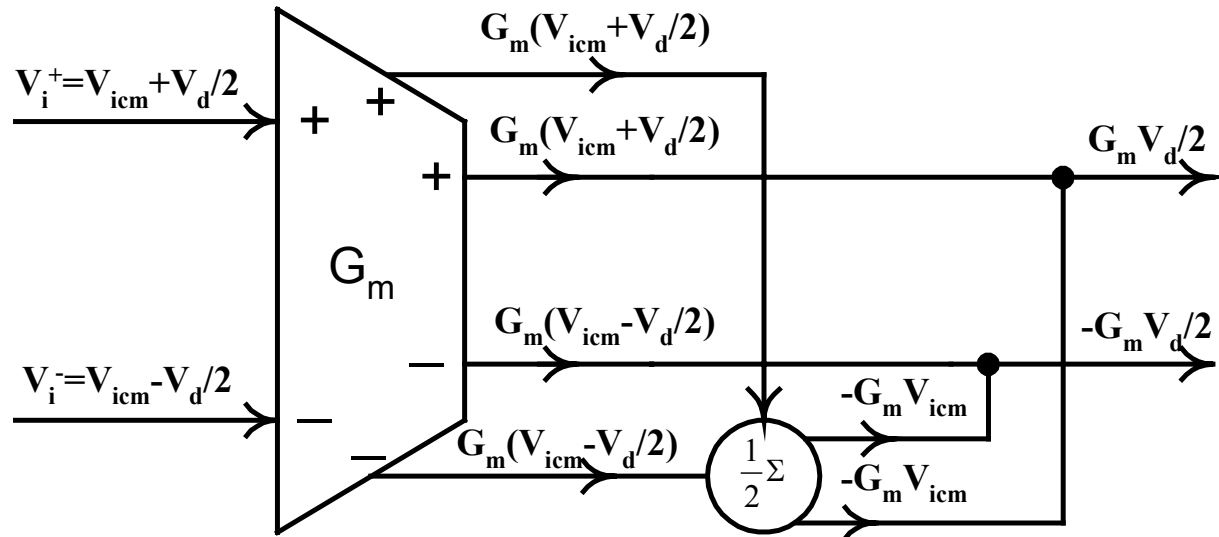
Common Mode OTA



Pseudo differential OTA With CMFF

- ✓ CMFF is applied to cancel the common mode input signal
- ✗ Add load to the driving stage, input capacitance doubles
- ✗ CMFB is still needed

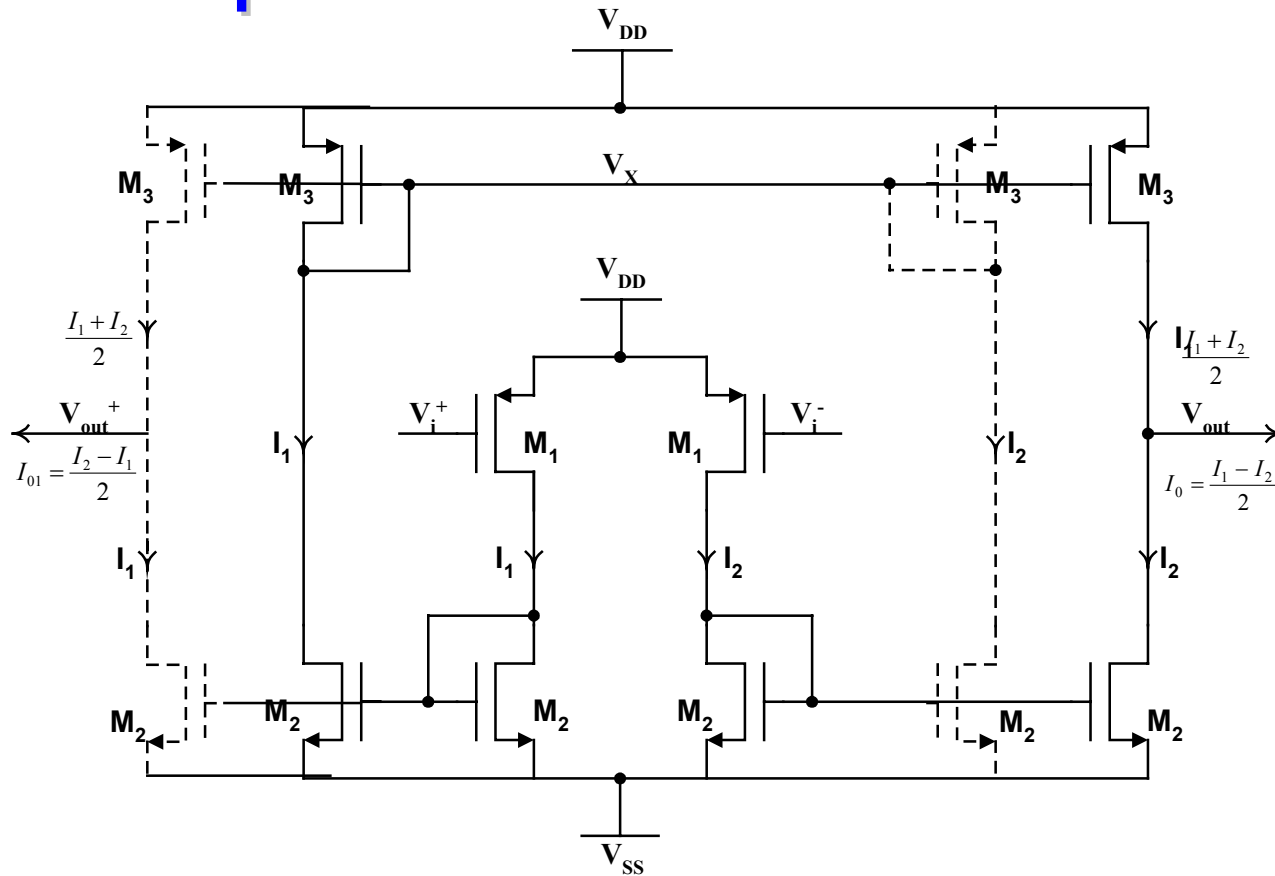
# Proposed OTA Block Diagram (solution 3)



- ❑ Common-mode detection using the same differential transconductance by making copies of the current
- ✓ Input capacitance is not increased
- ✓ CMFF is inherently achieved
- ✓ CMFB can be easily arranged

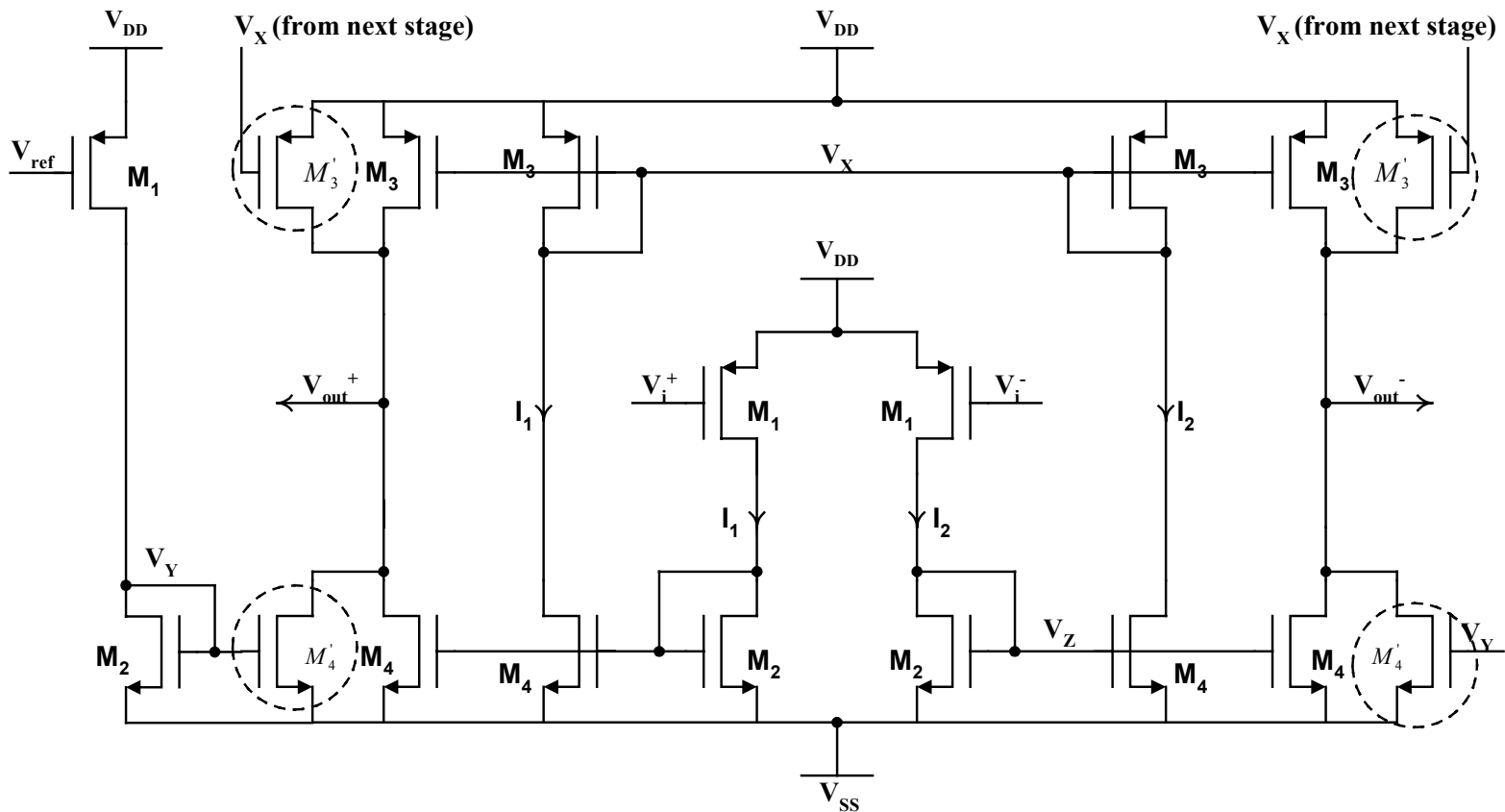
# How to Implement the Proposed OTA?

# Proposed OTA Architecture



- ❑ Inherent common-mode detection
- ❑ Inherent common-mode Feedforward

# Combine CMFB and CMFF



- ❑ CMFB is arranged exploiting the direct connection of the OTAs
- ❑ Avoid using a separate common-mode detector
- ❑ Differential-mode signals and common-mode signals share basically the same loop

# Small Signal Analysis

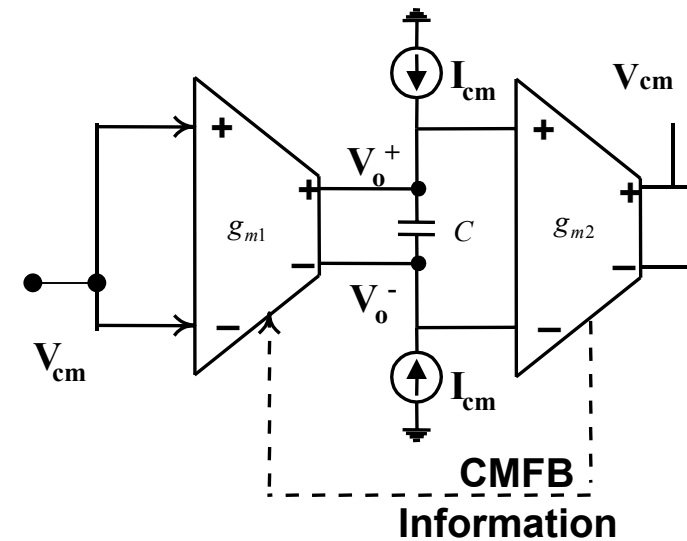
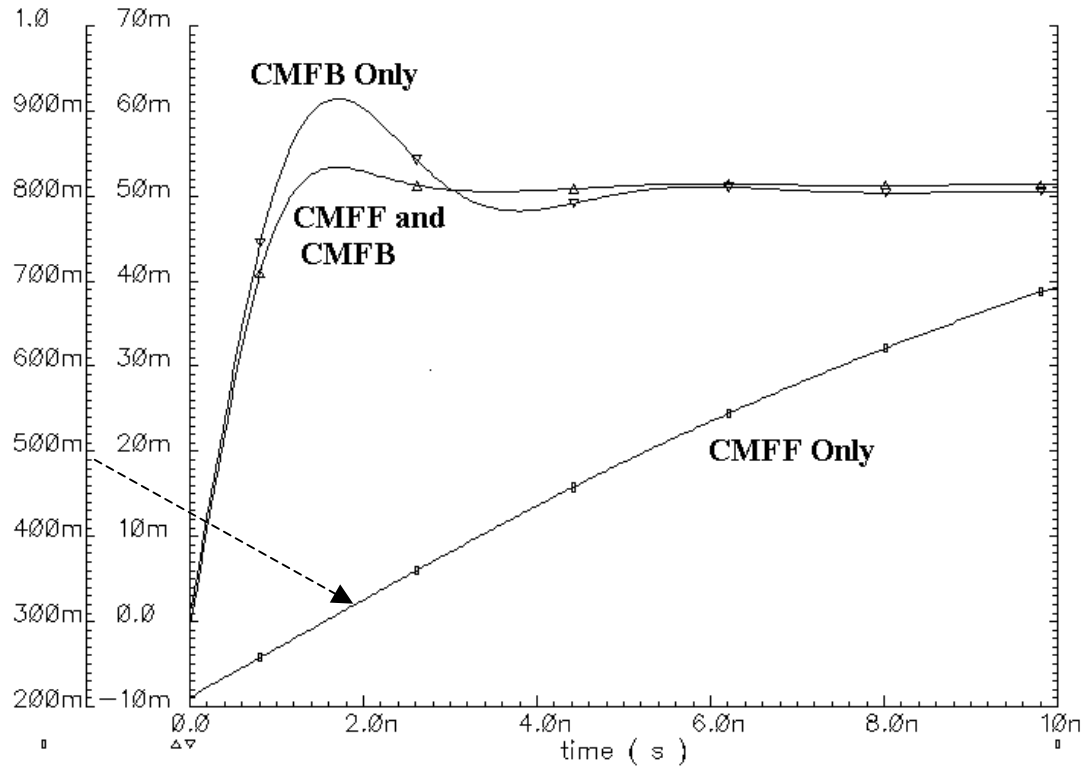
- ❑ The path from the differential signal to the output encounters one pole
- ❑ The other path is a common-mode path

$$g_m(s) = \frac{i_{od}}{v_d} \cong g_{m1} \frac{g_{m2}}{g_{m2} + sC_Z} = \frac{g_{m1}}{1 + s/\omega_{nd}} \quad \omega_{nd} = \frac{g_{m2}}{C_Z}$$

$$\Delta\phi \cong -\tan^{-1}(\omega / \omega_{nd1})$$

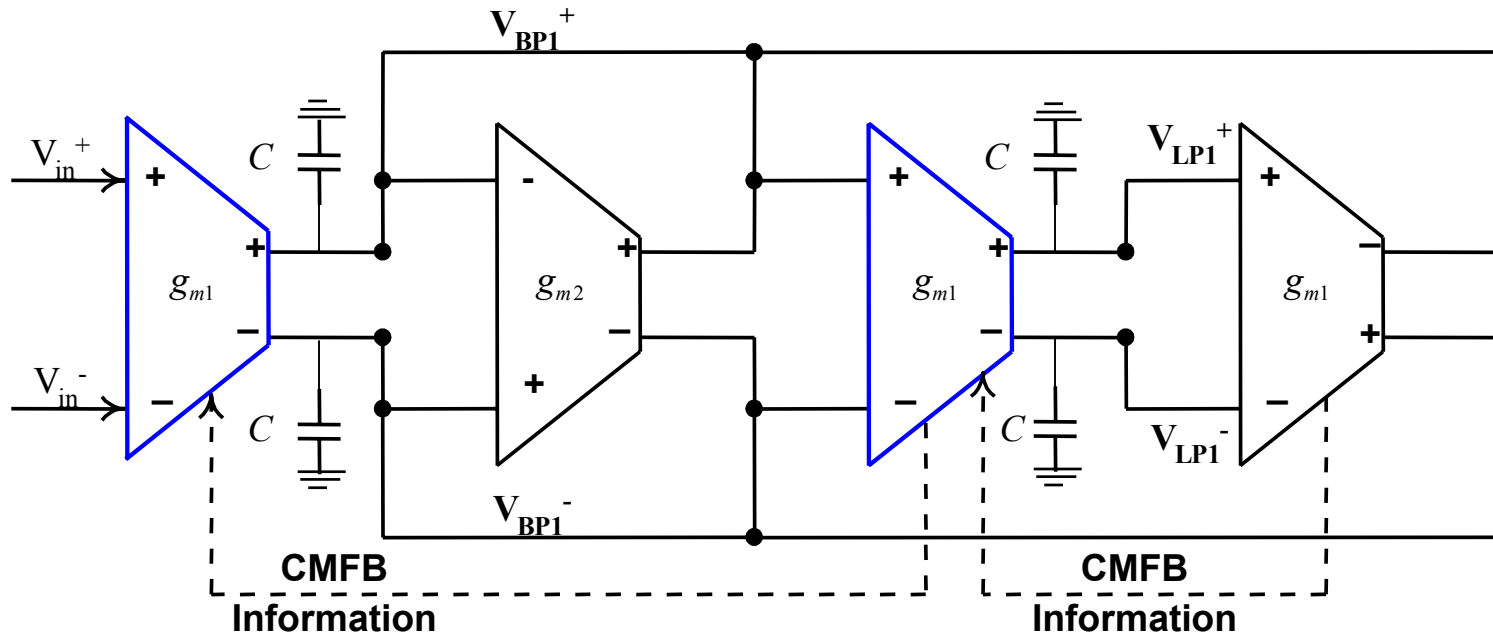
$$\min V_{DD} = \max \left\{ (V_{TN} + V_{ov1} + V_{ov2} + V_{peak}), (|V_{TP}| + V_{ov3} + V_{ov4}) \right\}$$

# Simulation Results



Output voltage applying common-mode current step ( $I_{cm}$ )

# How to use OTAs as CM Detector?



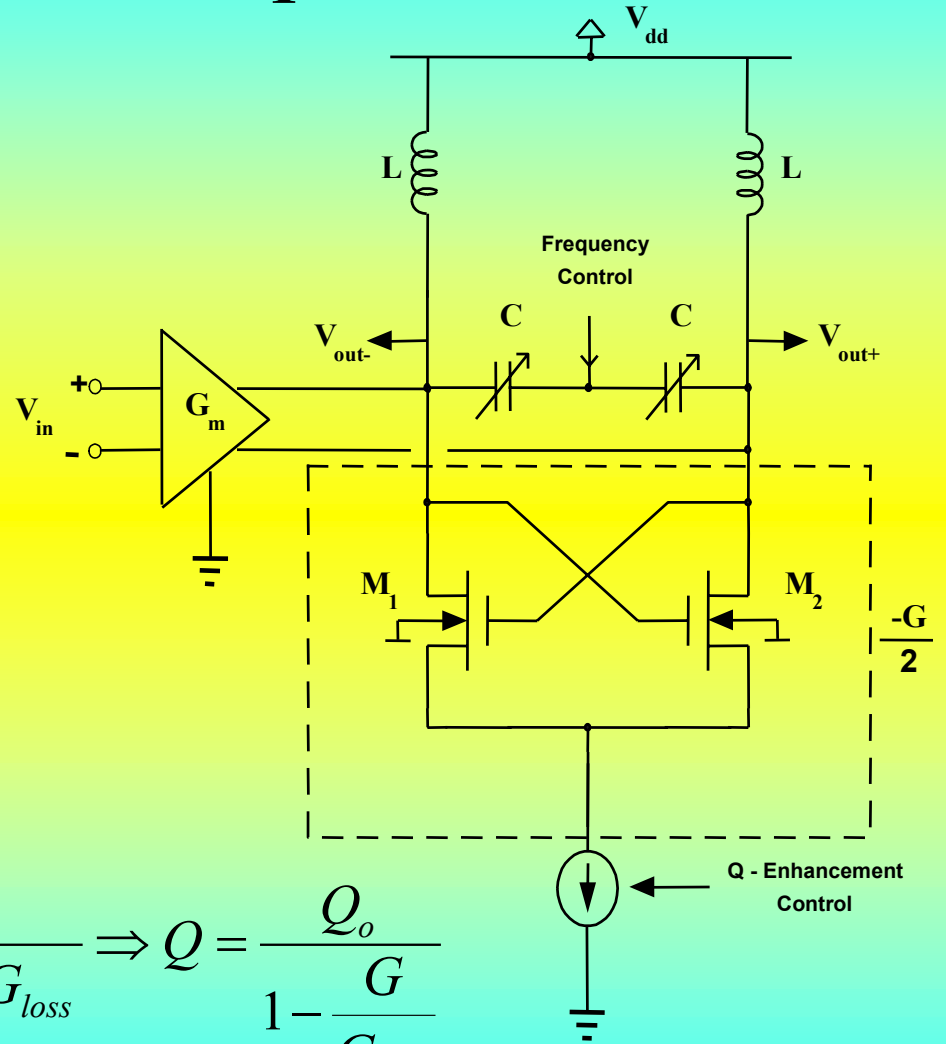
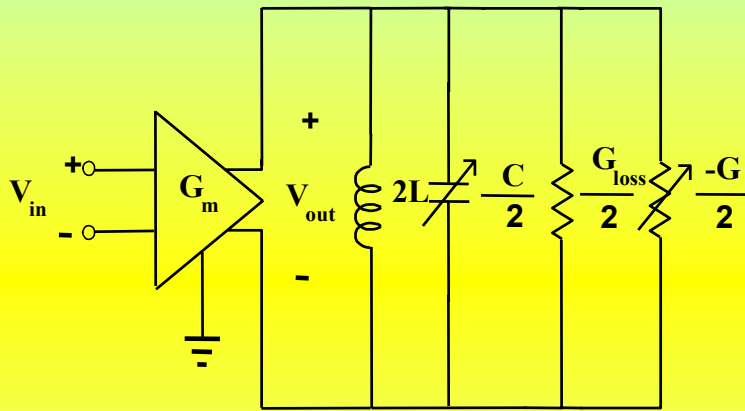
- ❑ A 2<sup>nd</sup> Order Filter is used as an example
- ❑ Exploit direct connection of the cascaded OTAs in the filter
- ❑ Differential OTA used as CM detector also



How to design filters operating  
in microwave frequencies ?



# Q-Enhancement Bandpass Filters



$$Q_o \equiv \frac{1}{\omega_o L G_{loss}} \Rightarrow Q = \frac{Q_o}{1 - \frac{G}{G_{loss}}}$$

(a)

$(G_{loss} > G \text{ for stability})$

(b)

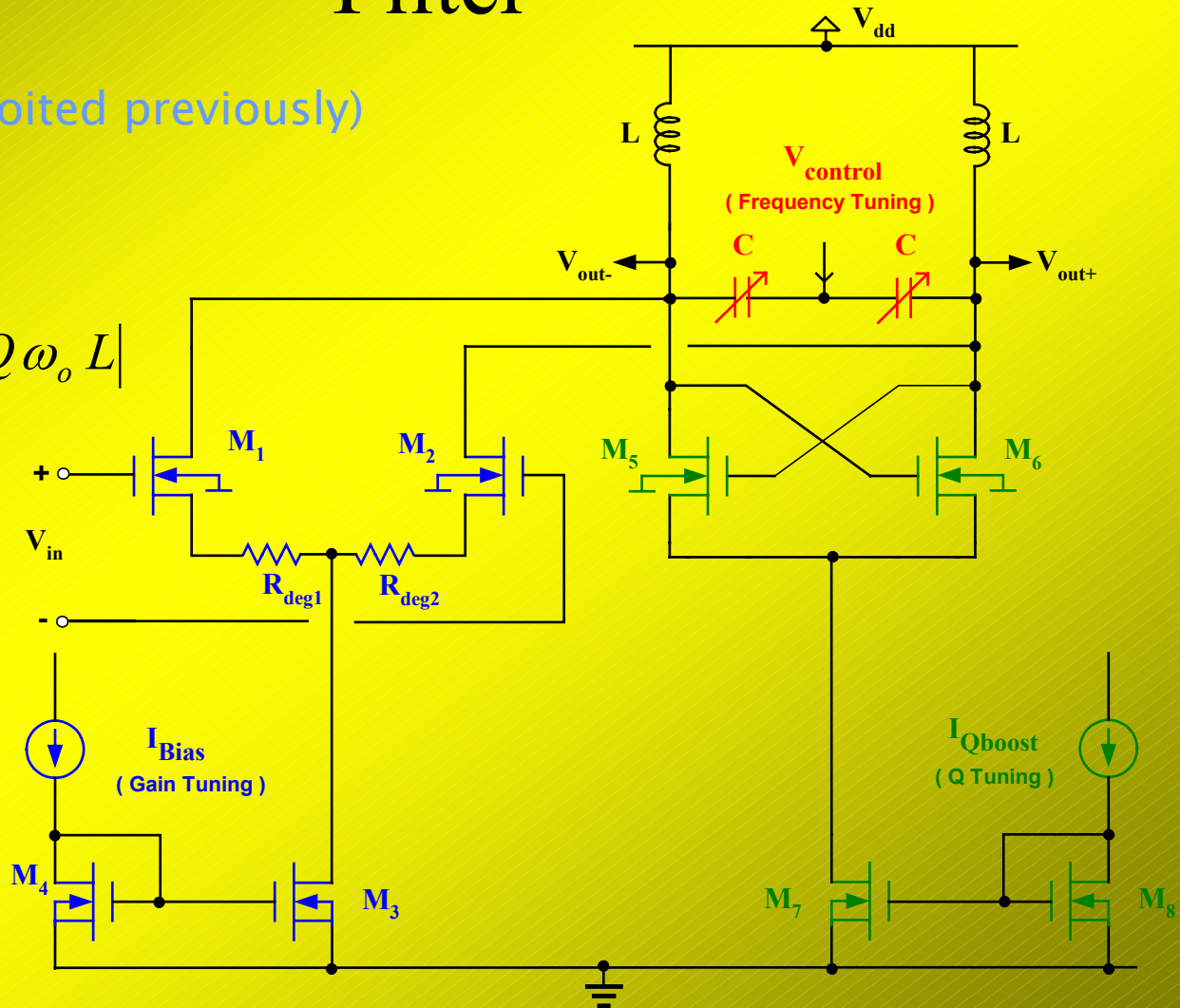
# A CMOS Programmable RF Bandpass Filter

Programmable in:

- Peak Gain (not exploited previously)
- Filter Q
- Center Frequency

$$|H(j\omega_o)| \cong |G_m(j\omega_o) Q \omega_o L|$$

$$\omega_o \cong \frac{1}{\sqrt{LC}}$$



# A CMOS Programmable Bandpass Filter

- The peak gain programmability through the input  $G_m$  stage.

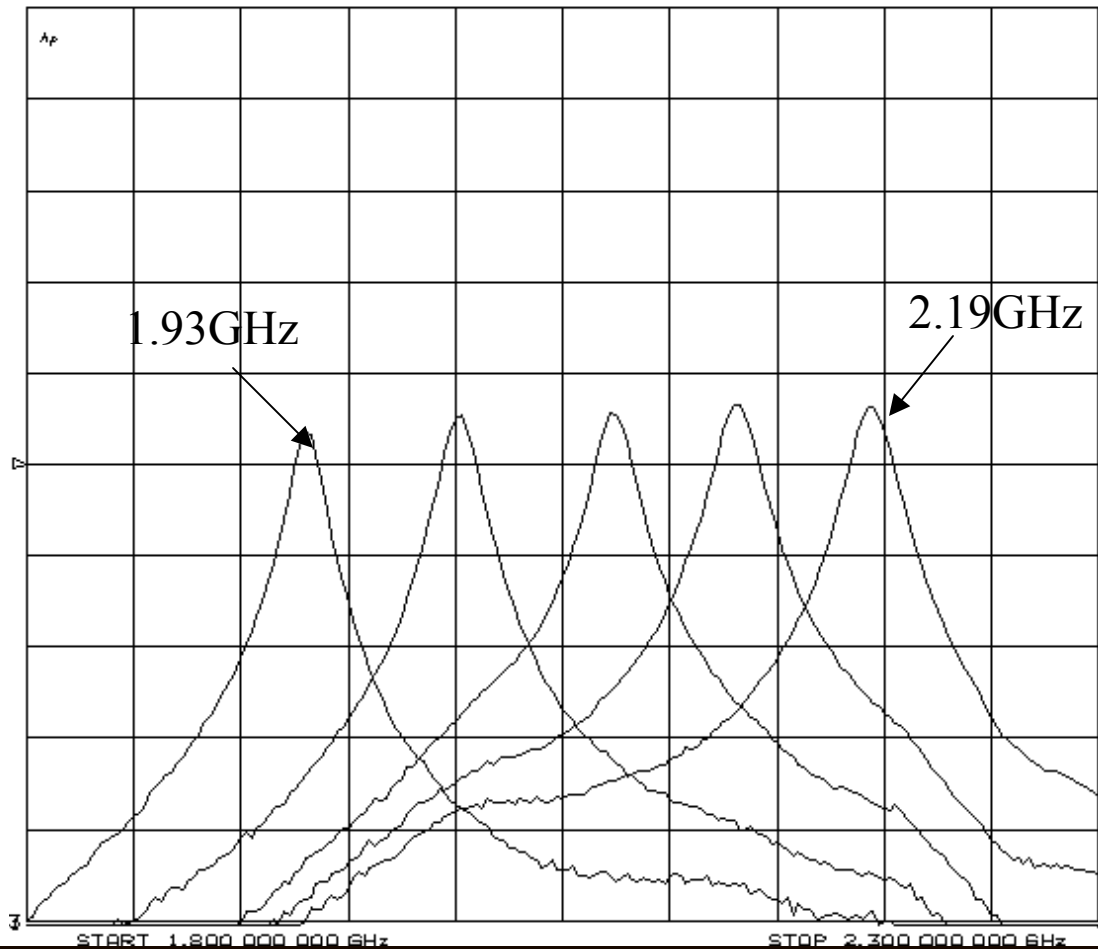
$$|H(j\omega_o)| \cong \left| \frac{G_m(j\omega_o)}{G_{loss} - G} \right| = |G_m(j\omega_o) Q \omega_o L|$$

- Increasing  $Q$  also increases the peak gain.
- If  $\omega_o$  and  $Q$  are fixed, the peak gain can be modified through  $G_m$ .



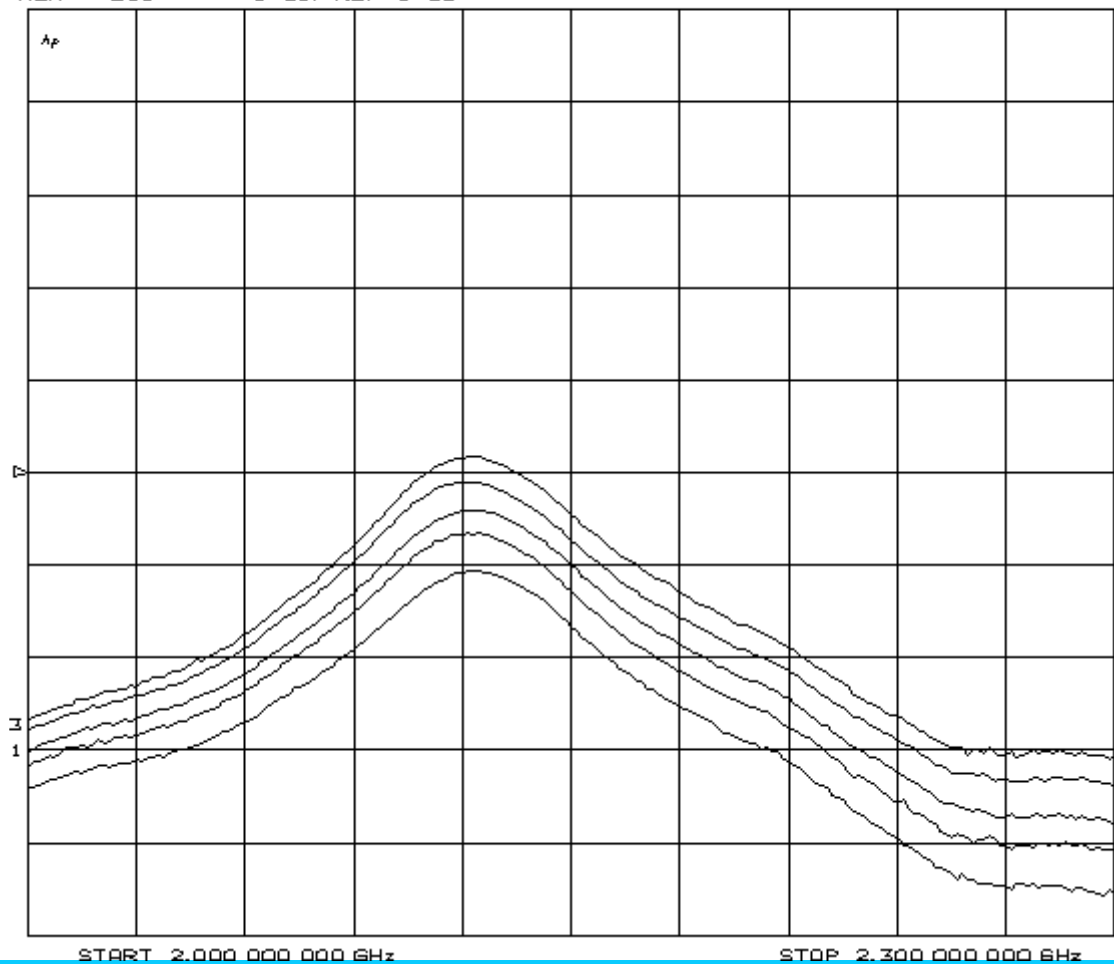
# Measured Frequency Tuning

13% around  
2.1GHz with  
 $Q \sim 100$



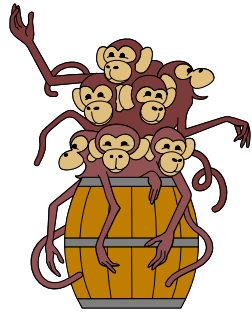
# Measured Peak Gain Tuning

Around  
2 octaves with  
 $f_o=2.12\text{GHz}$   
and  $Q=40$



Providing gain at the  $\omega_o$  of an image-reject filter is useful in a receiver front-end after the LNA, to relax the NF spec of the mixer.

Frequency- and Q-tuning  
techniques for OTA-C filters



# Need for Automatic Tuning

- Process variations can change  $f_0$  and  $Q$  by at least 20%
- Parameters also change with temperature and time(aging)
- Automatic tuning is a critical issue for the optimal performance of continuous-time circuits.

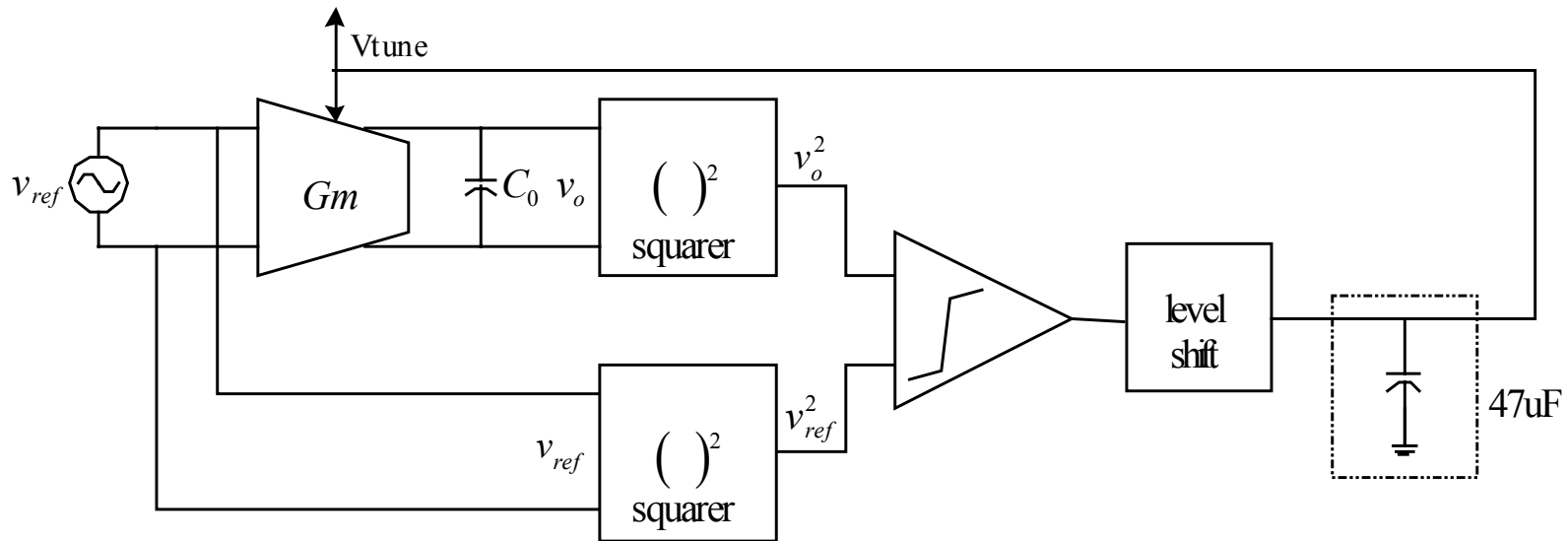
# Methods of tuning

- Master-Slave
- Based on trigonometric properties
- Based on filter phase information
- Pre-tuning
- Burst tuning
- Switching between two filters

# Automatic Frequency Tuning Scheme

BASED ON TRIGONOMETRIC FUNCTION PROPERTIES

$$\sin^2 x + \cos^2 x = 1$$

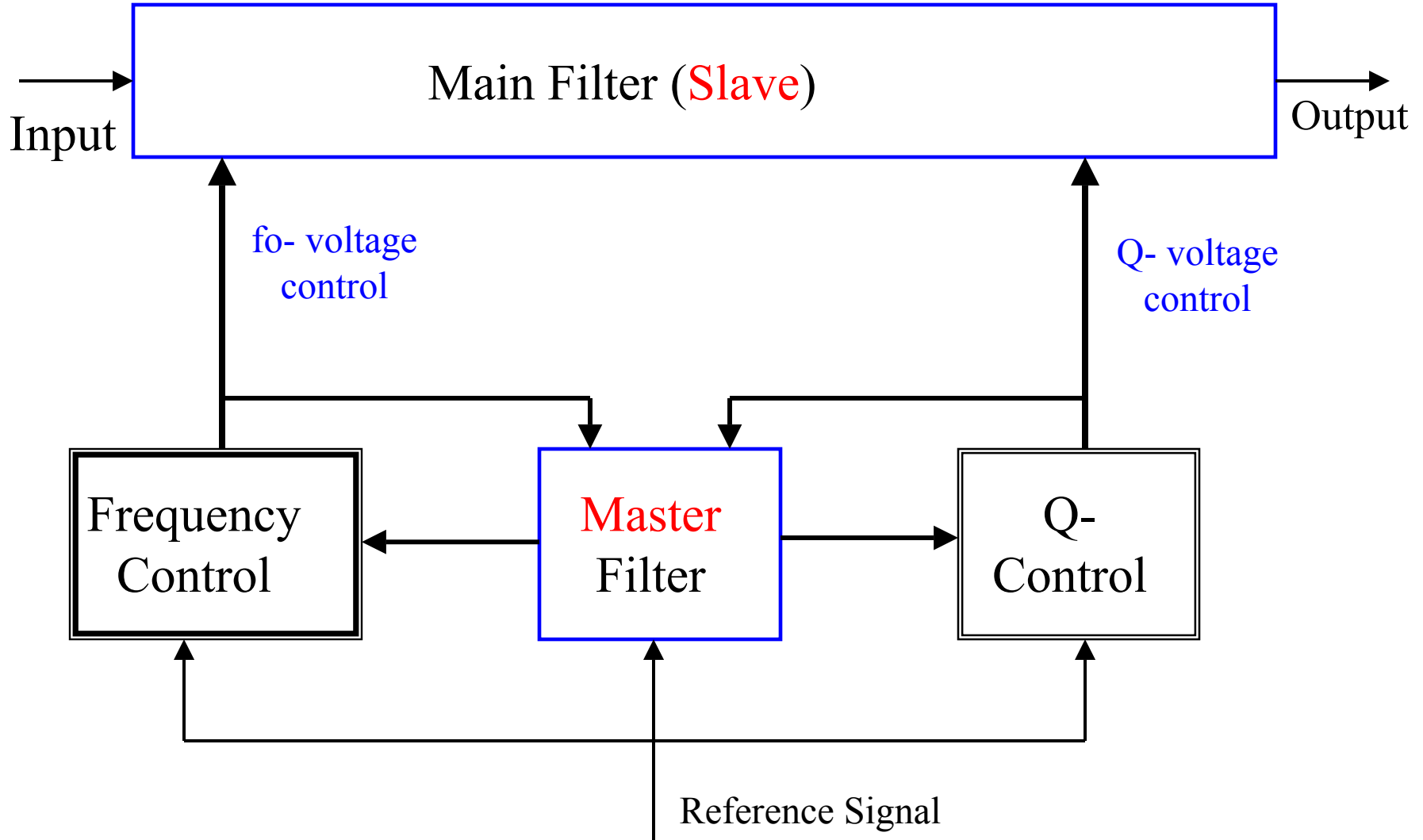


➤ Integrator--Gm & C: 
$$v_o^2 = \frac{1}{2} \left( \frac{f_u}{f_r} \right)^2 A^2 + \frac{1}{2} \left( \frac{f_u}{f_r} \right)^2 A^2 \cos(4\pi f_r t)$$

➤ Level shifter--Maximize the linear range of the automatic tuning system.

# Master-Slave Tuning Concept

## Master-Slave Tuning Concept



# Frequency Tuning

## Phased-Locked Loop (PLL)

- Most widely used scheme
- Accurate (less than 1% error is reported)
- **Square wave input reference**
- Only Phase - Frequency Detector, and LPF are the additional components
- It may take a large area overhead

VCF, VCO, Single OTA, Peak detect, adaptive....

# Q Tuning Schemes

Based on an envelope detector and a switched-capacitor integrator. It yields an accuracy of about 30%

## Modified LMS

- Q-accurate of about 1%
- It does not use envelope detector
- **Square wave input, any periodic function is sufficient**
- Independent of frequency tuning

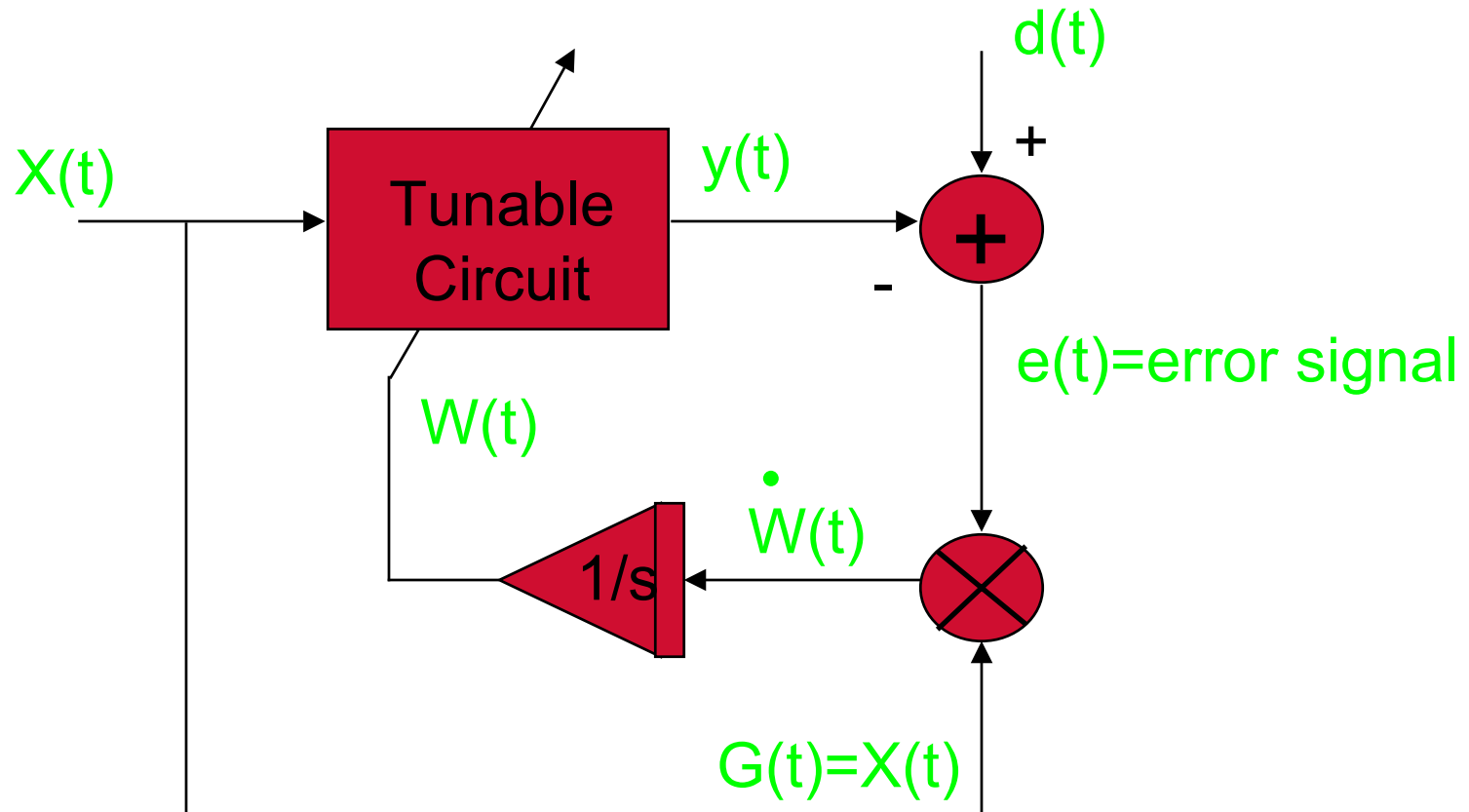
# Adaptive LMS Algorithm: Introduction

- Called Adaptive “Least-Mean-Squares” Algorithm because it learns by minimizing the mean-square error (MSE) between a desired response and the actual response of a system
- Minimizes error by updating system coefficients through a feedback loop

# Adaptive LMS Algorithm: Theory

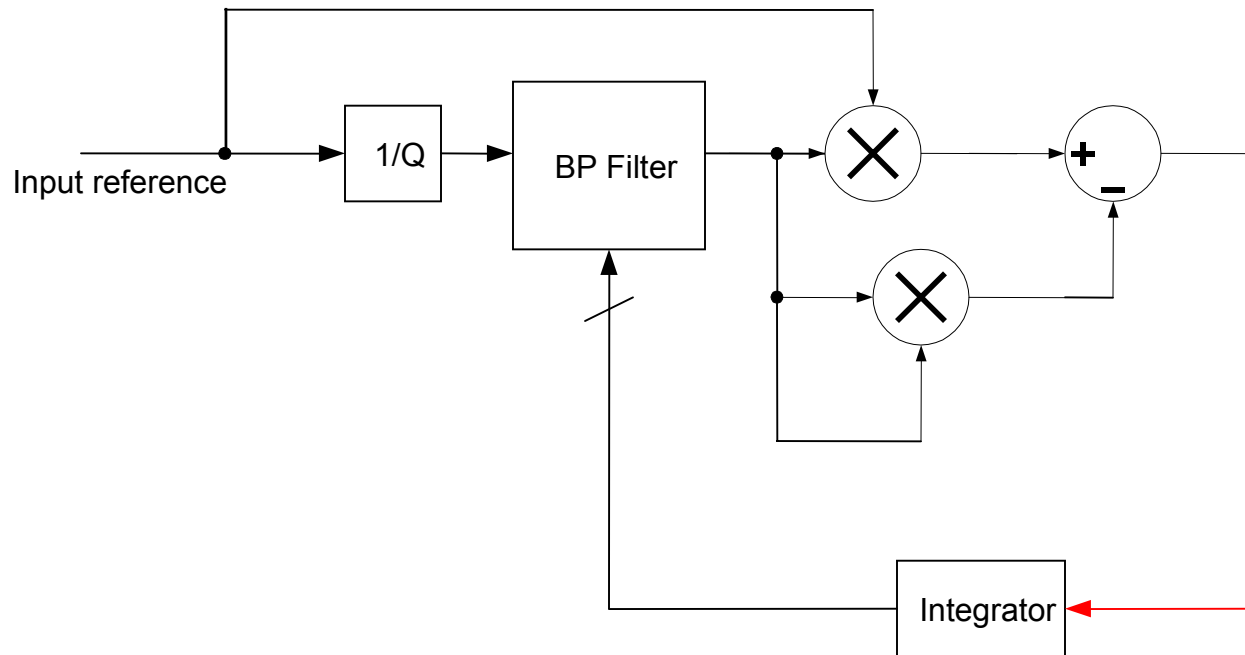
- Using the steepest descent algorithm to minimize the MSE we obtain:
- $\dot{\mathbf{W}}(t) = \mathbf{k}[\mathbf{d}(t) - \mathbf{y}(t)]\mathbf{G}(t) = \mathbf{k}[\mathbf{e}(t)]\mathbf{G}(t)$ 
  - $\mathbf{W}(t)$  = tuning signal
  - $\mathbf{d}(t)$  = desired system output
  - $\mathbf{y}(t)$  = actual system output
  - $\mathbf{G}(t)$  = tuning gradient (partial derivative of  $\mathbf{y}(t)$  with respect to  $\mathbf{W}(t)$ )
  - $\mathbf{k}$  = adaptation constant

# LMS Algorithm: Block Diagram (Linear System)



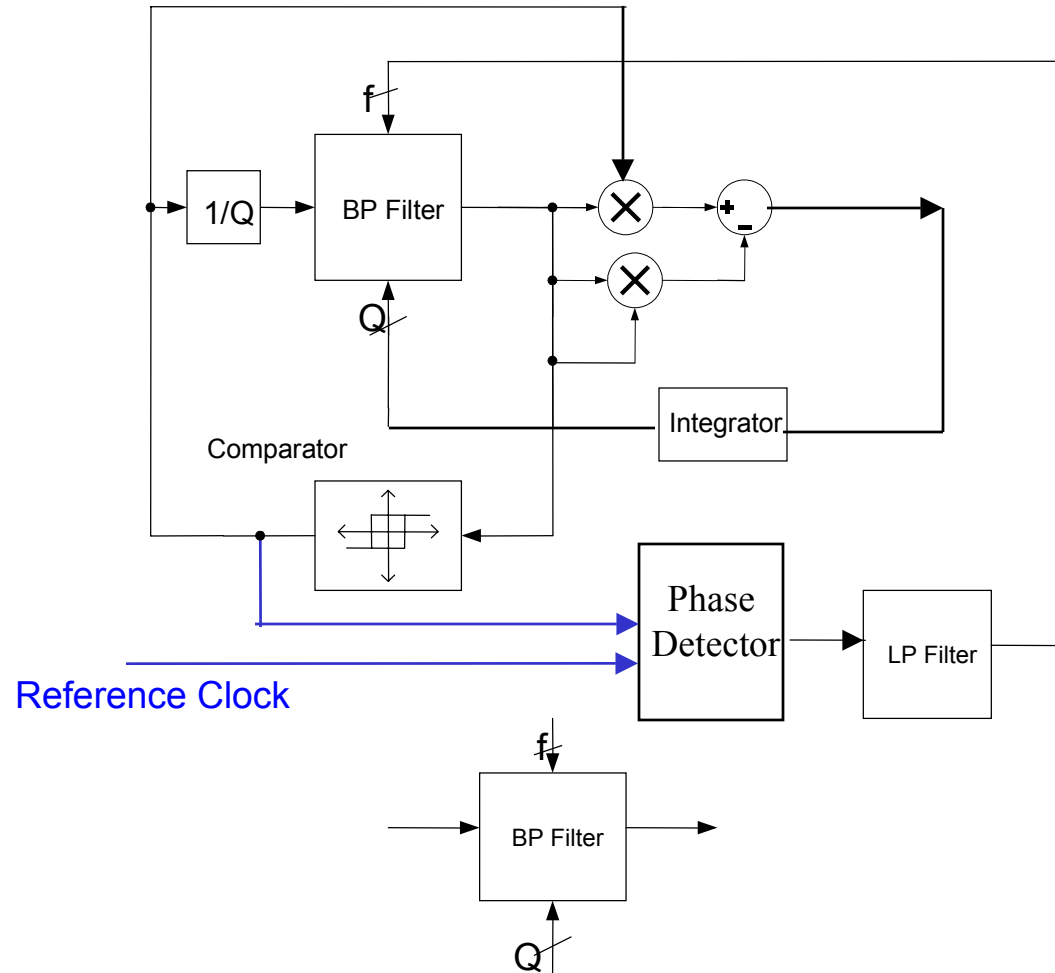


# An enhanced Q-tuning scheme



New implementation of modified-LMS Q-tuning scheme. Note that the LMS has been implemented in a different way yielding a structure with less offset voltages. See reference for more details.

# The enhanced tuning scheme

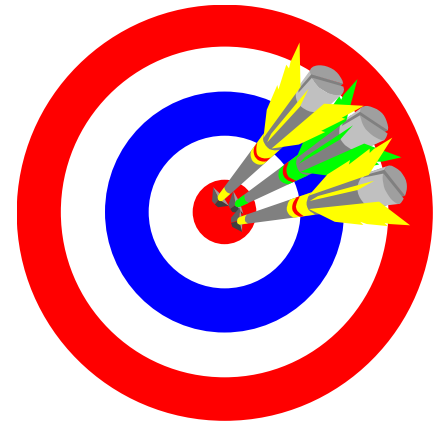


# Improvements over the previous Tuning scheme comparison

- Area overhead decreased

(Previous scheme => 2 extra filters

New scheme => 1 extra filter )



- Eases the matching restrictions

(Previous tuning scheme => match 3 filters

New tuning scheme => match 2 filters )

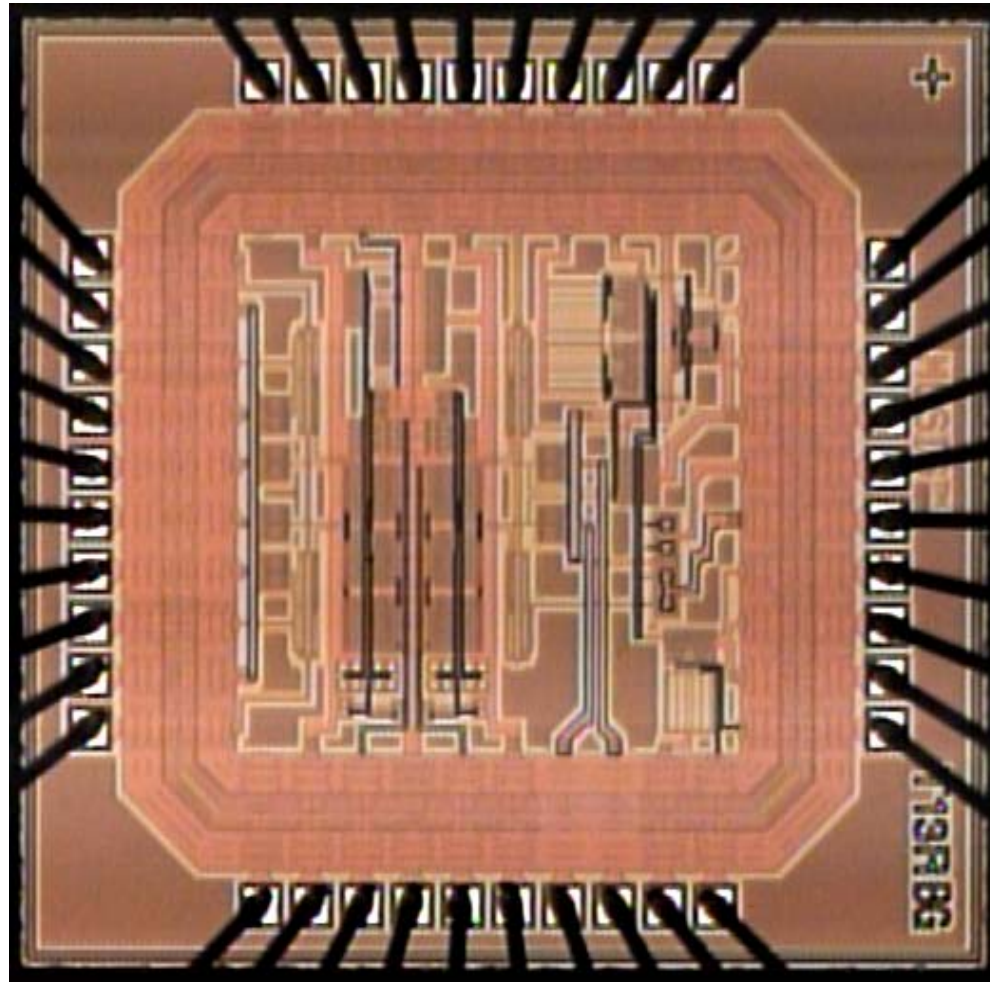
- Improves accuracy of tuning

(New tuning scheme is more tolerant to offsets than the previous one)

The Q-tuning loop speed can be equal to the f<sub>0</sub>-tuning loop for optimal performance



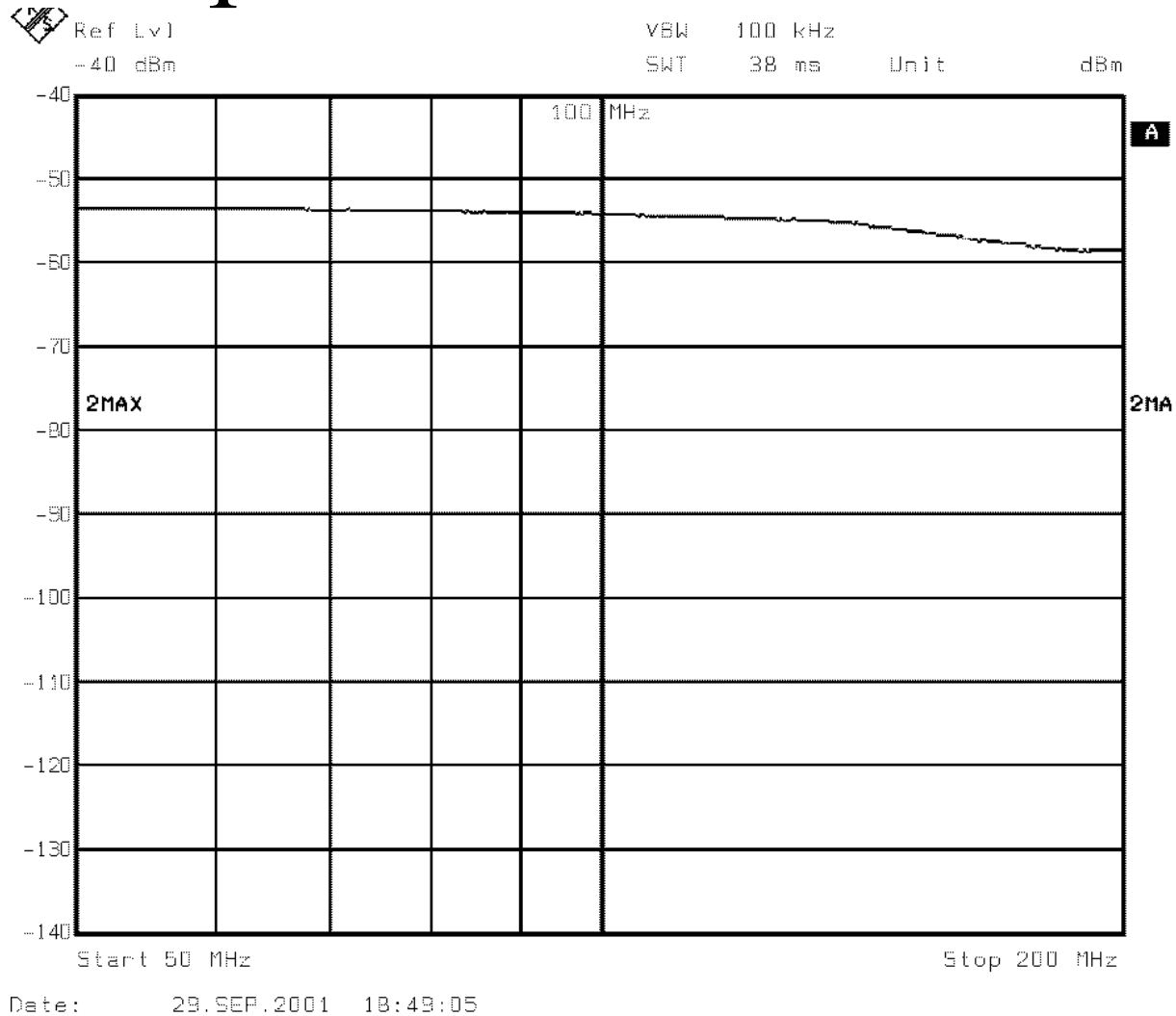
# Die Photograph



900um

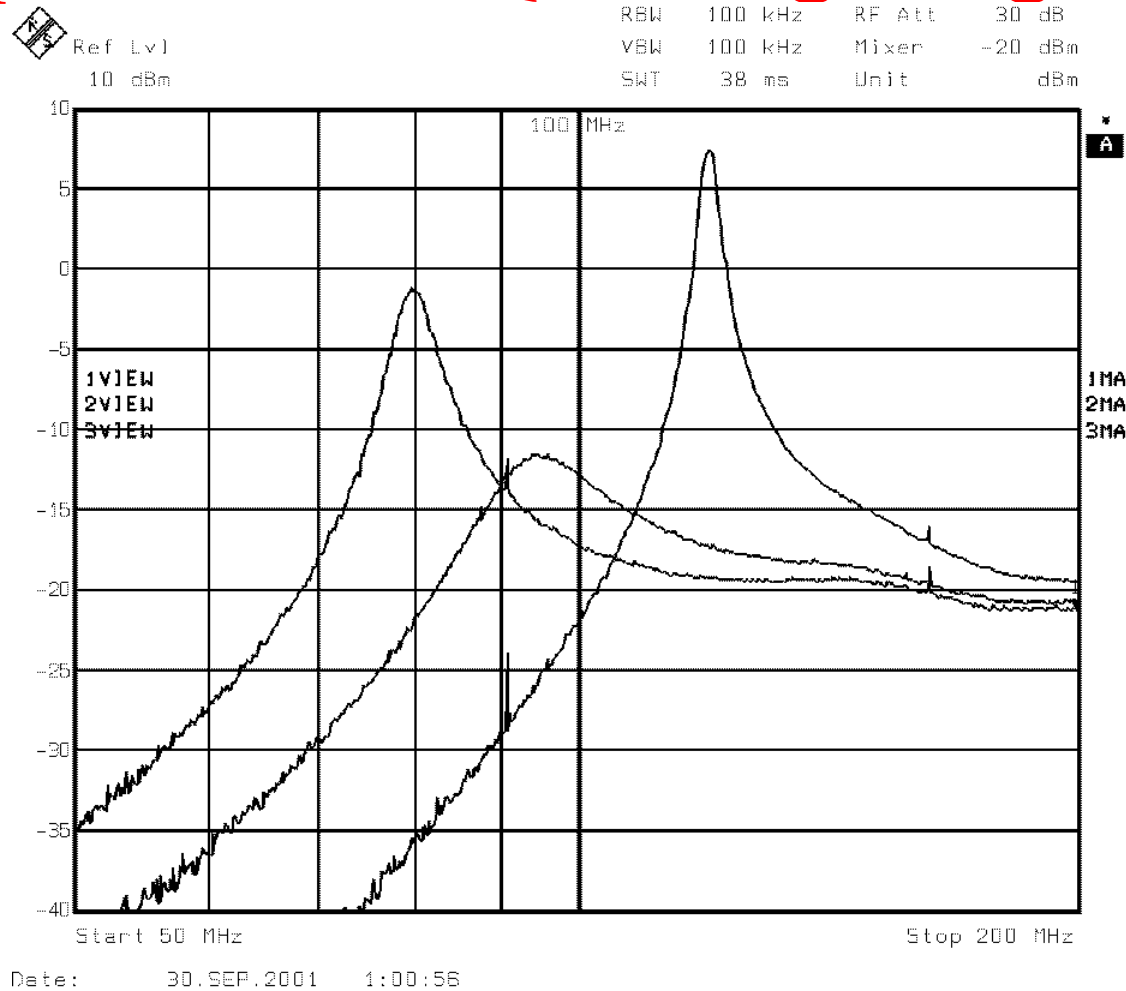
900um

# Experimental results on



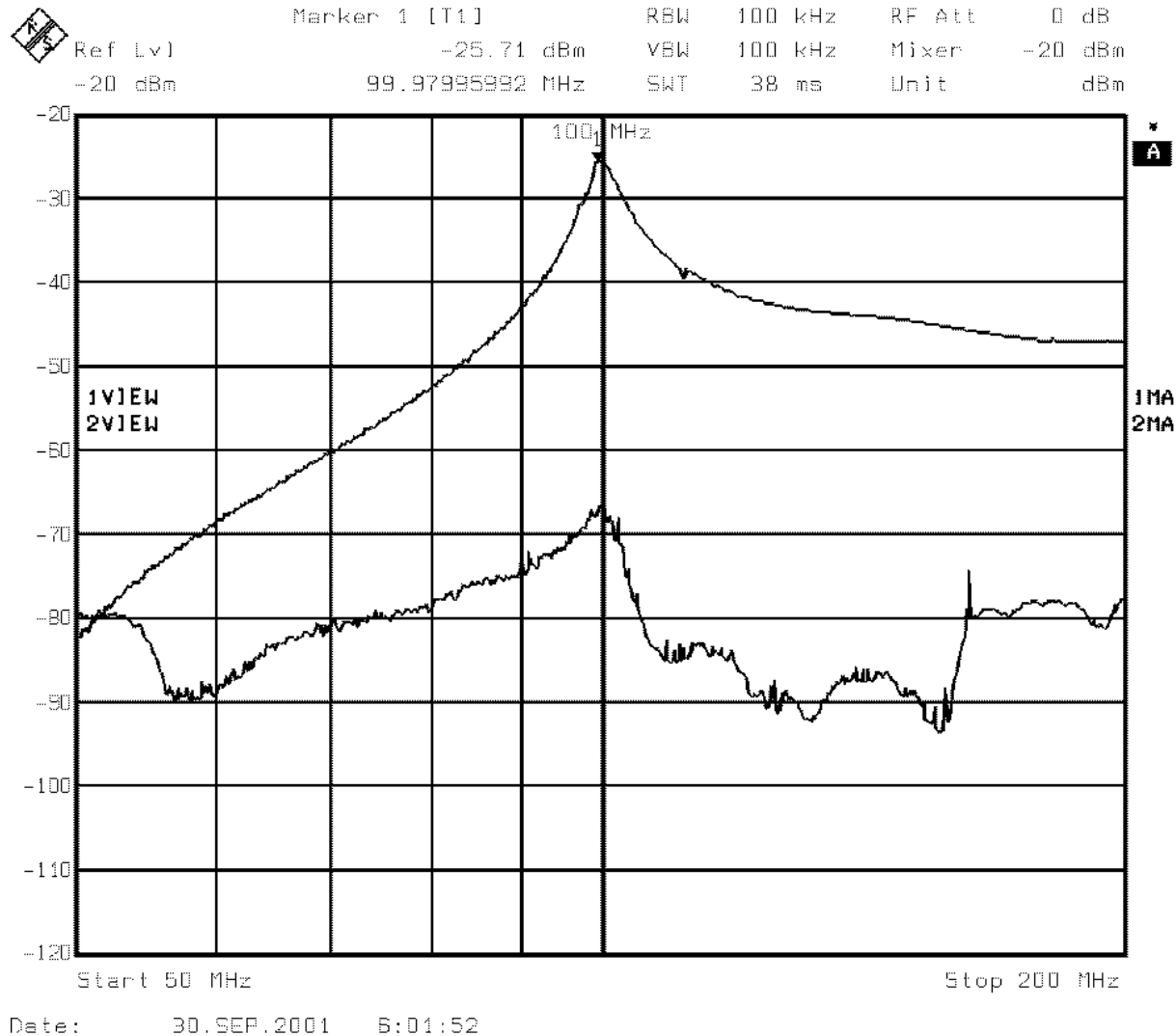
This response should be subtracted from other plots to get actual response

# Experimental Q tuning range results



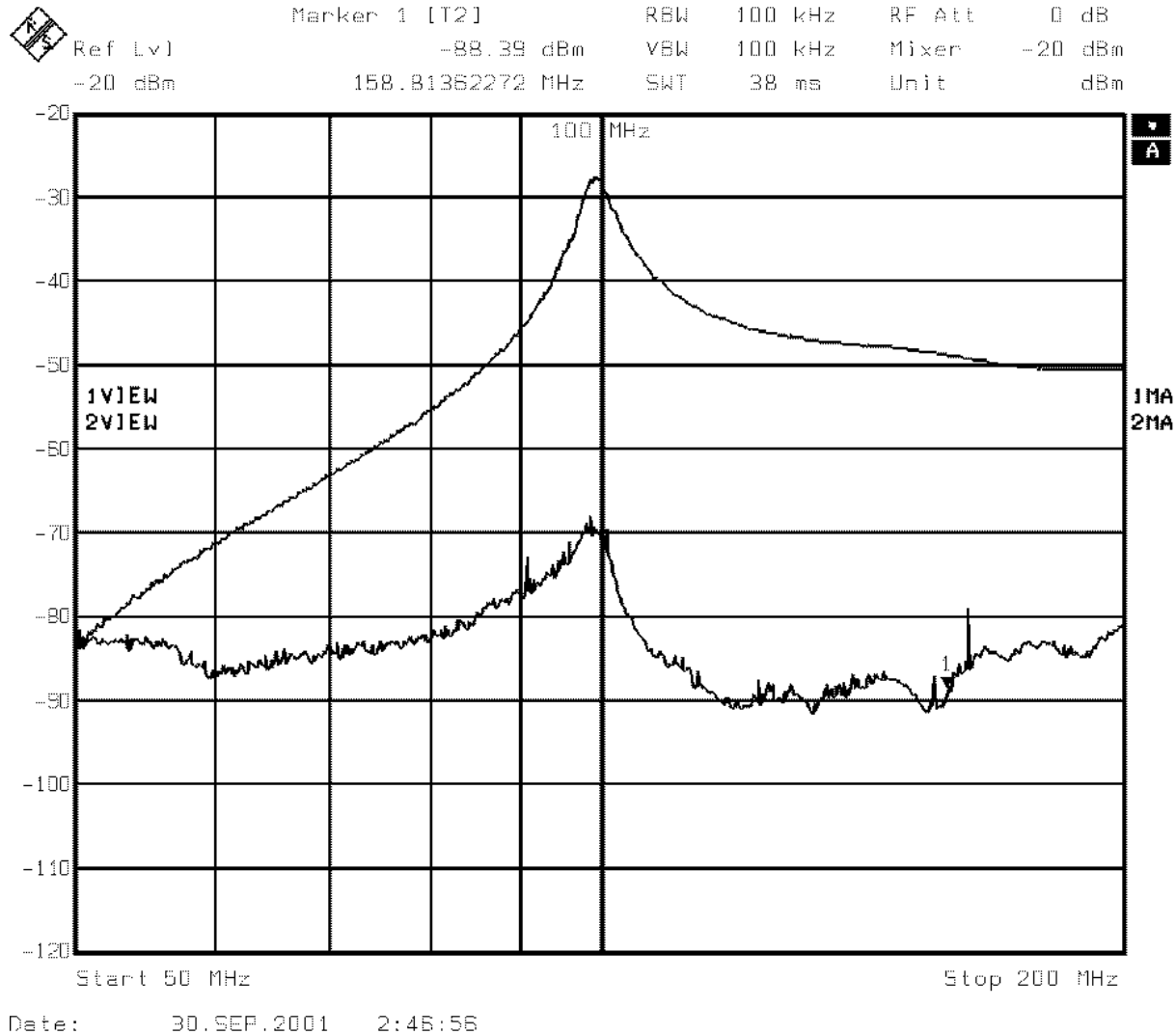
- Qs of 16, 5 and 40 at 80,95 and 110 MHz

# DM-CM response of the filter



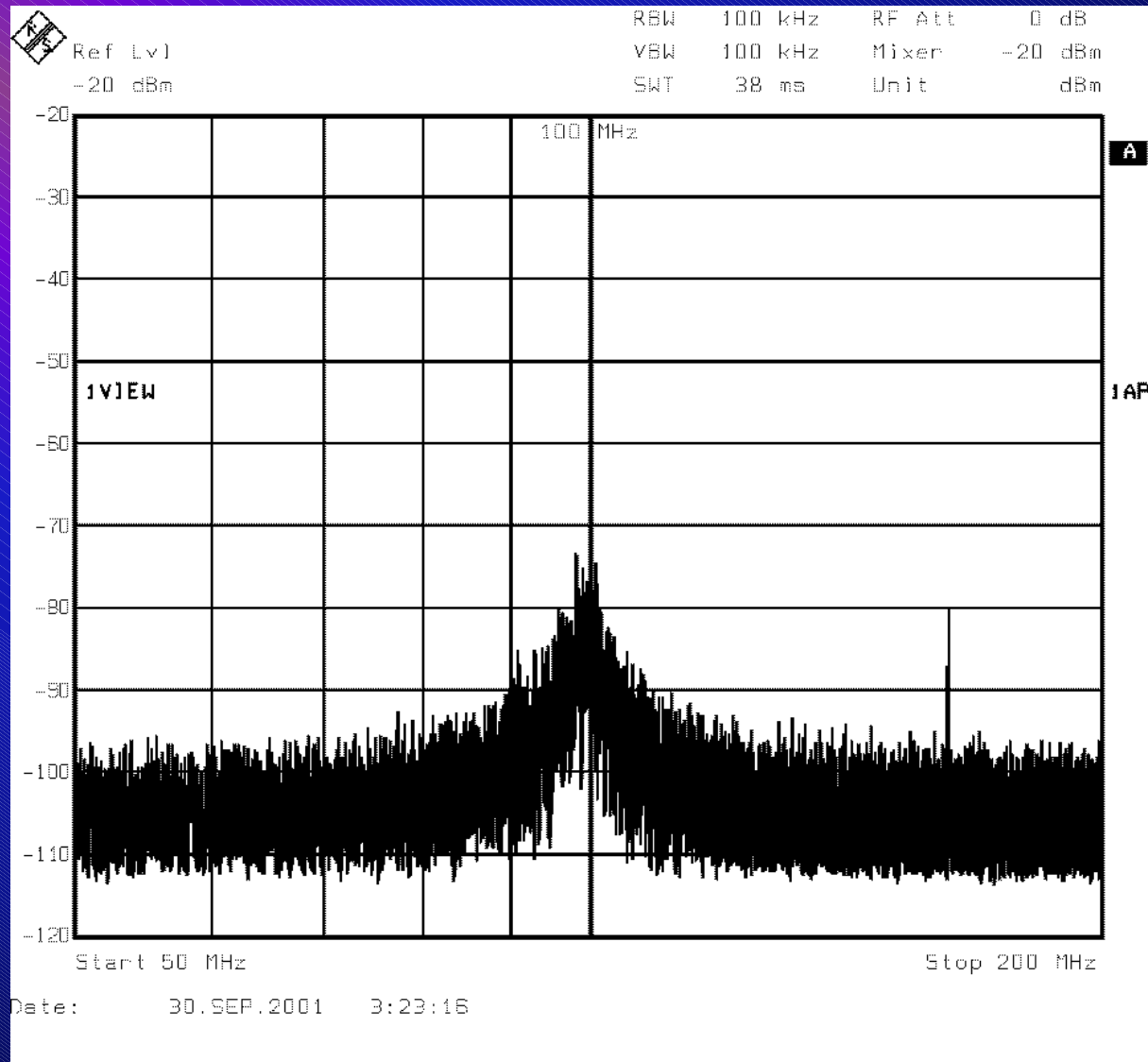
- CMRR is more than 40dB in the band of interest

# Supply response of the filter



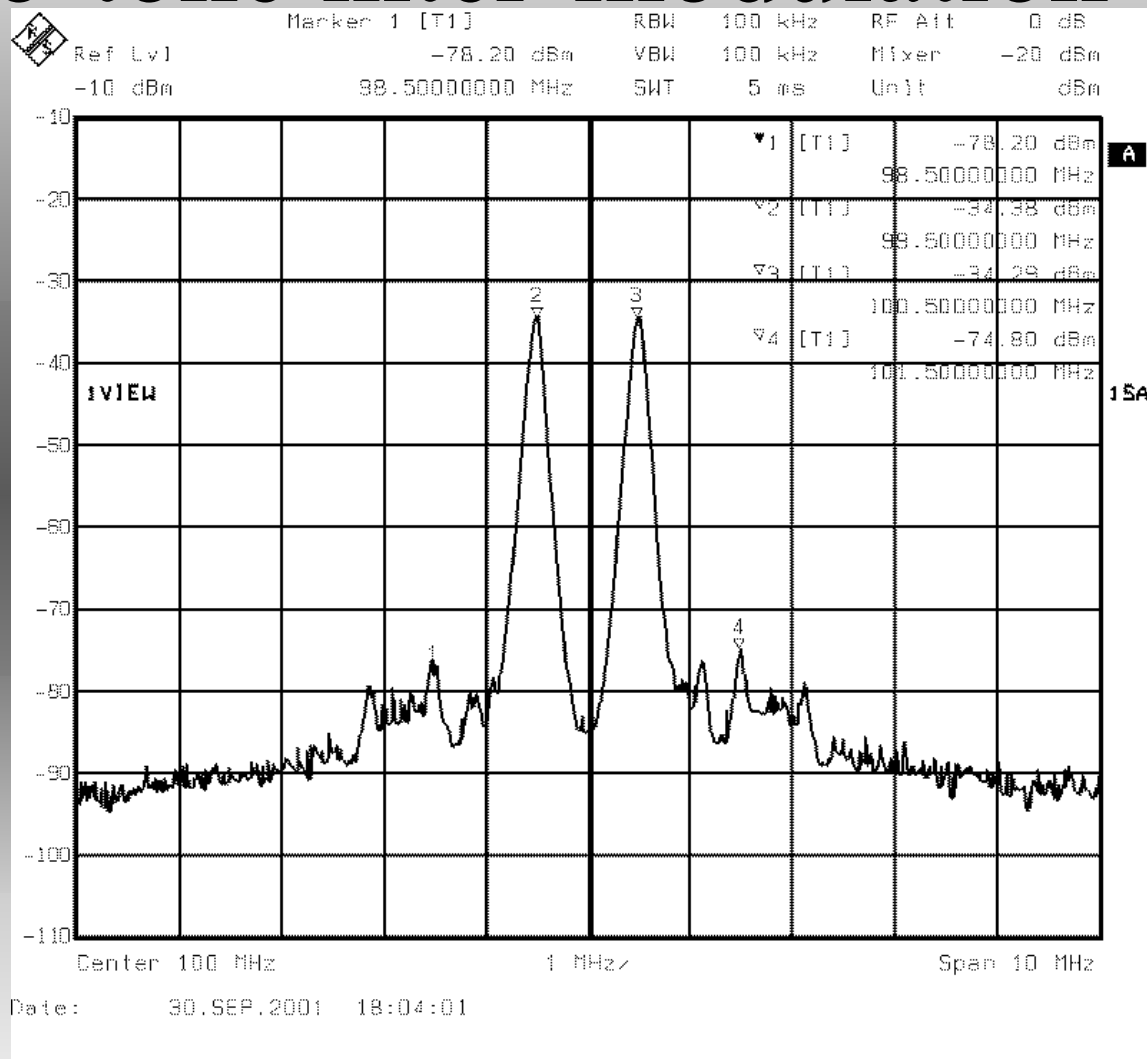
- PSRR- is more than 40dB in the band of interest

# Noise response of the filter



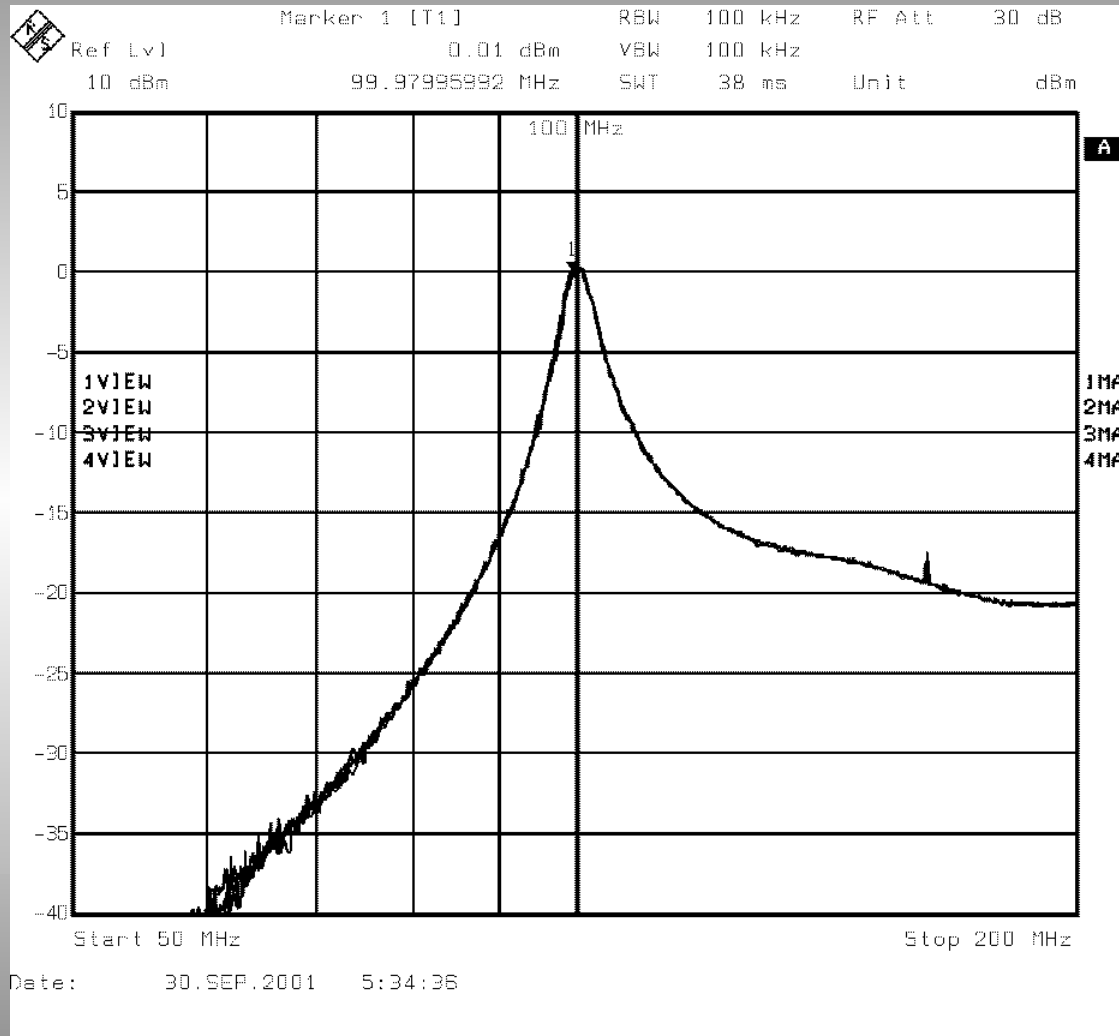
- Total integrated noise power at the output = -60dBm

# Two-tone inter-modulation test



- $IM_3$  of 45dB when the input signal is 44.6mV

# Filter response for four different ICs



- The tuning works!

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## References

- [1] C.F. Wheatley and H.A. Wittlinger, "OTA obsoletes OP AMP", *P. Nat. Econ. Conf.* pp. 152-157, Dec. 1969.
- [2] M. Bialko and R.W. Newcomb. "Generation of all finite linear circuits using Integrated DVCCS," *IEEE Trans. on Circuit Theory*, vol CT-18, pp.733-736, Nov. 1971.
- [3] S. Franco, "Use Transconductance Amplifier to make Programmable Active Filters," *Electronic Design*, vol 21, pp. 98-101, September 1976.
- [4] T. Deliyanis, "Active RC Filters Using Operational Transconductance Amplifier and Operational Amplifier," *Int. J. of Circuit Theory Appl.* Vol 8, pp. 39-54, Jan. 1980.
- [5] K.S. Tan, and P. Gray, "Fully-integrated analog filters using bipolar-JFET technology", *IEEE J. Solid-State Circuits*, SC-13, (6), pp. 814-821, 1980.
- [6] K. Fukahori, "A bipolar voltage-controlled tunable filter", *IEEE J. Solid-State Circuits*, SC-16, (6), pp. 729-737, 1981.
- [7] H.S. Malvar, "Electronically Controlled Active Filters with Operational Transconductance Amplifier," *IEEE Trans. Circuit Syst.*, vol CAS-29, pp. 333-336, May 1982.
- [8] H. Khorramabadi and P.R. Gray, "High Frequency CMOS Continuous-Time Filters," *IEEE J. Solid-State Circuits*, Vol. SC-19, no. 6, pp 939-948, December 1984.
- [9] A. Nedungadi and T.R. Viswanathan. "Design of Linear CMOS Transconductance Elements," *IEEE Trans. on Circuits and Systems*, Vol. 31, pp. 891-894, October 1984.

- [10] J.L. Pennock, "CMOS triode transconductor for continuous-time active integrated filters", *Electron. Lett.*, 21, pp. 817-818, 1985.
- [11] R. L. Geiger and E. Sánchez-Sinencio, "Active Filter Design Using Operational Transconductance Amplifiers: A tutorial", *IEEE Circuits and Devices Magazine*, vol 1, pp. 20-32, March 1985.
- [12] R.L. Geiger, and E. Sánchez-Sinencio, "Active filter design using operational transconductance amplifiers: a tutorial:", *IEEE Circuits Devices Mag.*, 2, (1). Pp. 20-32, 1985.
- [13] A. Nedungadi, and R.L. Geiger, "High frequency voltage controlled continuous-time low-pass filter using linearized CMOS integrators", *Electron. Lett.*, 22, pp. 729-731, 1986.
- [14] E. Seevinck, and R.F. Wassenaar, "A versatile CMOS linear transconductor/square-law function circuit", *IEEE J. Solid-State Circuits*, 22, pp. 366-377, 1987.
- [15] E. Sánchez-Sinencio, R.L. Geiger, and H. Nevarez-Lozano, "Generation of continuous-time two integrator loop OTA filter structures", *IEEE Trans. Circuits Syst.*, 35, pp. 936-946, 1988.
- [ 16] F. Krummenacher and N. Joehl. " A 4 MHZ CMOS Continuous-Time Filter with On- Chip Automatic Tuning," *IEEE J. Solid-State Circuits*, vol. 23, pp. 750-758, June 1988.

- [17] A. Brambila, G. Espinosa, and E. Sánchez-Sinencio, “Noise optimization in operational transconductance amplifier filters”, *Proceedings of IEEE ISCAS 89*, Vol. 4, pp. 118-121, 1989.
- [18] S.N. Filho, M.C. Schneider, and R.N.G. Robert, “New CMOS OTA for fully integrated continuous-time circuit applications”, *Electron. Lett.*, 25, (24), pp. 1674-1675, 1989.
- [19] P.M. VanPeteghem, and R. Song, “Tuning strategies in high-frequency integrated continuous-time filters”, *IEEE Trans. Circuits Syst.*, 36, (1) pp. 1163-1166, 1990.
- [20] K.A. Kozma, D.A. Johns, and A.S. Sedra, “An adaptive tuning circuit for integrated continuous-time filters”, *Proceedings of IEEE ISCAS*, pp. 1163-1166, 1990.
- [21] J. Silva-Martínez, M.S.J. Steyaert, and W. Sansen, “A large signal very low-distortion transconductor for high-frequency continuous-time filters”, *IEEE J. Solid-State Circuits*, 26, pp. 946-955, 1991.
- [22] J. Silva-Martínez, M. Steyaert, and W. Sansen, “A Novel approach for the automatic tuning of continuous-time filters”, *Proceedings IEEE International Symposium on Circuits and Systems*, pp. 1451-1455, 1991.
- [23] G.A. Deveirman, and R.G. Yamasaki, “A 27 MHz programmable bipolar 0.05° equiripple linear-phase lowpass filter”, *Proceedings of IEEE ISSCC-92*, pp. 64-65, 1992.

- [24] J.E. Kardontchik, "Introduction to the design of transconductance-capacitor filters", (*Kluwer Academic Publishers*), Boston, 1992.
- [25] J. Ramírez-Angulo, and E. Sánchez-Sinencio, "Programmable BiCMOS transconductor for capacitor-transconductance filters", *Electron. Lett.*, 28, pp. 1185-1187, 1992.
- [26] W.M. Snelgrove, and A. Shoval, "A balanced 0.9  $\mu\text{m}$  CMOS transconductance-C filter tunable over the VHF range", *IEEE J. Solid-State Circuits*, 27, pp. 314-312, 1992.
- [27] J. F. Duque-Carrillo, "Control of the common-mode component in CMOS continuous-time fully differential signal processing in Analog integrated circuits and signal processing", (*Kluwer Academic Publishers*), pp. 131-140, 1993.
- [28] A. Wysynski, "Low-voltage CMOS and BiCMOS triode transconductors and integrators with gain enhanced linearity and output impedance", *Electron. Lett.*, 30, (3), pp. 211-212, 1994.
- [29] A. Wysynski, and R. Schaumann, "Avoiding common-mode feedback in continuous-time  $G_m C$  filters by use of lossy integrators", *Proceedings of IEEE ISCAS 94*, pp. 281-284, 1994.
- [30] J.-Y. Kim, and R.L. Geiger, "Characterisation of linear MOS active attenuator and amplifier", *Electron. Lett.*, 31, pp. 511-513, 1995.
- [31] F. Rezzi, A. Baschirotto, and R. Castello, "A 3V 12-55 MHz BiCMOS pseudo-differential continuous-time filter", *IEEE Trans. Circuits Syst. I, Fundam. Theory Appl.*, 42, pp. 896-903, 1995.

- [32] S.L. Smith, and E. Sánchez-Sinencio, “Low voltage integrators for high-frequency CMOS filters using current mode techniques”, *IEEE Trans. Circuits Syst. II, Analog Digit. Signal Process.*, 43, pp. 39-48, 1996.
- [33] G. Efthivoulidis, L. Toth, and Y.P. Tsvividis, “Noise in Gm-C filters”, *IEEE Trans. on Circuits Syst. II, Analog Digit. Signal Process.*, 45, (3), pp. 295-302, 1998.
- [34] J.M. Stevenson, and E. Sánchez-Sinencio, “An accurate quality factor tuning scheme for IF and high-Q continuous-time filters”, *IEEE J. Solid-State Circuits*, 33, pp. 1970- 1978, 1998
- [35] T. Itakura, T. Ueno, H. Tanimoto, and T. Arai, “A  $2 V_{pp}$  linear input-range fully balanced CMOS transconductor and its application to 2.5V 2.5 MHz Gm-C LPF”, *Proceedings of IEEE CICC*, pp. 509-512, 1999.
- [36] S. Solis-Bustos, J. Silva-Martínez, F. Maloberti, and E. Sánchez-Sinencio, “A 60dB Dynamic Range CMOS Sixth-Order 2.4MHz Low-Power Filter for Medical Applications,” *IEEE Trans. on Circuits and Systems-II*, Vol 47, No. 12, pp. 1391-1398, December 2000.
- [37] A. Veeravalli, E. Sánchez-Sinencio, and J. Silva-Martínez, “Transconductance amplifier structures with very small transconductances: A comparative design approach”, *IEEE J. Solid-State Circuits*, Vol. 37, No. 6, pp. 530-532, May 23 2002.

- [38] B. Provost and E. Sánchez-Sinencio, “On-chip ramp generators for mixed-signal BIST and ADC Self-Test”, accepted *IEEE J. Solid-State Circuits*.
- [39] P. Kallam, E. Sánchez-Sinencio, and A.I. Karesilayan, “An enhanced adaptive Q-tuning scheme for a 100 MHz fully-symmetric OTA-Based Filter”, accepted *IEEE J. Solid-State Circuits*.
- [40] F. Dülger, E. Sánchez-Sinencio, and J. Silva-Martínez, “A 1.3V 5mw, fully-integrated tunable bandpass filter at 2.1GHz in 0.35 $\mu$ m CMOS”, accepted for publication *IEEE J. Solid-State Circuits*.
- [41] A.N. Mohieldin, E. Sánchez-Sinencio, and José Silva-Martínez, “A fully balanced pseudo differential OTA with common-mode feedforward and inherent common-mode feedback detector”, accepted for publication *IEEE J. Solid-State Circuits*.