

current that a mirror diameter less than $\sim 8 \mu\text{m}$ was required to maintain STM operation.

Discussion: The factors affecting the MSR in these lasers can be calculated by generalising the treatment for longitudinal modes in edge-emitting lasers [4] to multiple transverse mode oscillation in surface emitters. The result is

$$\frac{P_1}{P_0} = \frac{a}{1 + bP_0} \quad (1)$$

$$a = \left(\frac{\Gamma_1}{\Gamma_0} \right) \left(\frac{1 - R_{21}}{1 - R_{20}} \right) \left(\frac{R_{10} R_{20}}{R_{11} R_{21}} \right)^{1/4} \quad (2)$$

$$b = \frac{2(R_{10} R_{20})^{1/4} \tau_s (\delta g + \delta \alpha)}{1 - R_{20} \Gamma_0 \gamma N A_0 h \nu} \quad (3)$$

where P_0 is the main mode power, P_1 is the secondary mode power, Γ_m is the confinement factor, γ is the spontaneous emission factor, R_{1m} and R_{2m} are the mirror reflectances, N is the carrier concentration, A_0 is the main mode area, τ_s is the carrier lifetime, $h\nu$ is the photon energy, δg and $\delta \alpha$ are the difference in modal gain and cavity loss, respectively, between the main mode and the secondary (higher order transverse) mode, and m is the mode index ($m = 0, 1$ here.) Eqns. 1–3 predict that the MSR should increase with increasing main mode power, and the effect should be greater for larger gain and cavity loss discrimination δg and $\delta \alpha$. The gain discrimination in these lasers is affected by both the position of the main mode with respect to the spectral gain peak (determined by the optical period of the Bragg mirrors and the roundtrip cavity phase), and the wavelength separation between modes (determined by the cavity aspect ratio.) The loss discrimination is determined by differences in diffraction loss and mirror reflectivity; the partially ordered output mirror provides a smaller reflectance for the higher order transverse modes because a larger fractional power is contained in the disordered, low reflectance region. In principle the amount of gain and loss discrimination can be determined by fitting eqns. 1–3 to the experimental results; we have found that in our devices the MSR increased with optical output power more rapidly above laser threshold than predicted. This could be due to the increasing gain discrimination experienced by higher order transverse modes at higher bias current; as the wavelength for peak spectral gain becomes longer than the lasing wavelength (which is the cause of the output power limitation) the spectral gain profile is less flat and δg increases.

Conclusions: We have studied the lateral mode control properties of VCSELs with a partially disordered epitaxial output mirror. Stable STM operation is maintained for mirror diameters less than $\sim 8 \mu\text{m}$. Laser threshold is larger for larger mesa size and smaller mirror diameter. Output efficiency for the present structure is low, but it is expected that the efficiency can be improved with a low dose ion implantation step for current confinement. This structure allows for single transverse mode operation with a lower series resistance than can probably be achieved using ion-implantation-induced gain guiding alone.

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MIN-NET WINNER-TAKE-ALL CMOS IMPLEMENTATION

Y. He and E. Sánchez-Sinencio

Indexing terms: Neural networks, Circuit theory and design

A charge-based winner-take-all (WTA) circuit is proposed. This WTA circuit is a min-net capable of selecting the minimum value among its input nodes and gives only one low voltage for the corresponding output node. The charge-based circuit uses a power supply of 3V, with low power dissipation due to the lack of static DC current involved. The WTA circuit is used in associative neural networks.

Introduction: The winner-take-all circuit is one of the fundamental sublayers in artificial neural network systems. Its application can be found among others, in the Hamming net [1], the Kohonen net [2] and the ART1 [3]. In these types of network, a set of weight vectors are usually encoded somehow in the system memory, thus when a stimuli vector is applied at the input, comparisons between this stimuli vector and the weight vectors will be conducted and the results of the comparisons are represented by a measurement called dissimilarity. Assuming that the encoded weight vectors are represented by

$$W^i = \{w_1^i, w_2^i, \dots, w_n^i\} \quad i = 1, 2, \dots, m \quad (1)$$

and the stimuli input is represented by

$$X = \{x_1, x_2, \dots, x_n\} \quad (2)$$

the dissimilarity of the i th weight vector D_i is defined as the summation of the difference between each bit of W^i and X , i.e.

$$D_i = \sum_{k=1}^n |x_k - w_k^i| \quad (3)$$

Another common name used for the dissimilarity is the Euclidean-based [4] distance. Note that for one stimuli input vector, several dissimilarity scores result, and the minimum dissimilarity, D_{min} , should be differentiated. This minimum dissimilarity provides a distance measurement between the stimuli input and the closest weight vector, i.e. the corresponding weight vector has the maximum similarity with the stimuli input. This minimum dissimilarity or maximum similarity selecting function, as a fundamental function in a competitive neural network, is performed by the WTA circuit.

Several WTA circuits have been reported [4–6], including our previous work [7, 8]. However, all those reported circuits are min-nets [1] and are based on selecting maximum input signals, therefore some kind of transformation has to be made to express the dissimilarity as a similarity. Note that the dissimilarity D_i and similarity S_i are related by $S_i = C - D_i$, where C is a constant. In this Letter, we represent a WTA circuit (min-net) which directly finds the minimum value among its analogue inputs. This is an extended version of the

WTA first reported in Reference 4. As mentioned above, it can be used to select the minimum dissimilarity score in associative neural networks.

WTA circuit implementation: Fig. 1 shows a three input-output WTA circuit (the input-output number can be

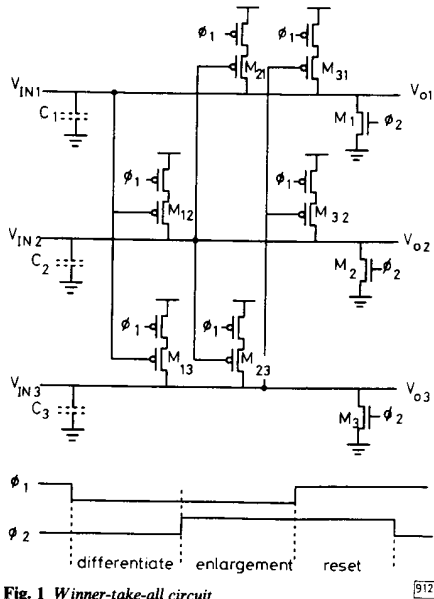


Fig. 1 Winner-take-all circuit

extended to any number as needed), where C_1 , C_2 and C_3 are parasitic capacitances, and the pMOS transistors M_{ij} are crosscoupled with each other. The first subscript (i) of M_{ij} indicates the gate node, and the second subscript (j) indicates the drain node. The subscript (ij) therefore represents the connection between node i and node j . The pMOS transistors on the top of M_{ij} are used as switches. The operation of the circuit is explained as follows: the input voltages are initially dumped onto the equal input parasitic capacitors (C_1 , C_2 and C_3), and those voltages serve as the initial gate voltages of the pMOS transistors (M_{ij}). During ϕ_1 (ϕ_1 becomes low), all the switches controlled by ϕ_1 are closed and the sources of the transistors M_{ij} are connected to power supply V_{DD} . The input capacitors (C_1 , C_2 and C_3) are therefore charged by V_{DD} through transistors M_{ij} . Because transistors M_{ij} are all cross-coupled, the charging of the capacitors operates in a competitive way. The node with a smaller voltage makes other pMOS transistors more conductive, the corresponding drain voltages therefore have faster rising rates, while the node with a larger voltage makes other pMOS transistors less conductive, and the corresponding drain voltages therefore have a smaller rising rate. As a result of this competition, only one node which corresponds to the smallest input voltage stays just one pMOS threshold voltage below the power supply ($V_{DD} - |V_{TP}|$), while all other nodes are charged to the power supply V_{DD} . This process can be called a differential process.

We have now differentiated the minimum input node from the others, represented by a voltage less than $V_{DD} - |V_{TP}|$. A greater difference between the minimum and other voltages is usually required. That is, to have a binary output (V_{DD} or 0 V). One practical option is to use an nMOS transistor clocked by ϕ_2 as a switch for each node. Note from Fig. 1 that ϕ_2 and ϕ_1 are overlapped clock phases. When ϕ_1 is low and ϕ_2 is high, the node voltages are further amplified. As long as the sizes of those nMOS transistors are smaller than the sizes of the pMOS transistors, the nodes with the voltages of V_{DD} will remain near constant, while the nodes with voltage less than $V_{DD} - |V_{TP}|$ will be pushed to ground voltage, due to the crosscoupled pMOS transistor interactions. This event is called the enlargement process. After the enlargement process,

all the node voltages are reset to ground, to process new inputs.

One practical characteristic of this circuit is the fact that the input parameter can be either an input voltage or an input capacitance. For instance, taking the capacitance as the input parameter, the capacitors are first discharged by a common voltage (say ground), then the WTA circuit will select the node with the maximum input capacitor and set the corresponding output node to a low voltage.

Fig. 2 shows the HSPICE simulation of the proposed WTA circuit. The first two plots illustrate ϕ_1 and ϕ_2 , and the plot at the bottom shows the V_{o1} , V_{o2} and V_{o3} time response. The

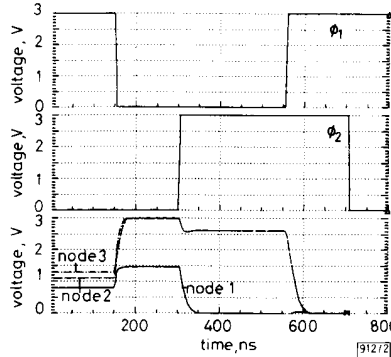


Fig. 2 HSPICE simulation of proposed WTA circuit

pMOS transistor sizes are $W/L = 3/2$, and the nMOS pull-down transistors sizes are $W/L = 3/15$. All substrates of the pMOS are tied to V_{DD} , and the substrates of the nMOS are tied to ground. The input voltages are $V_{in1} = 0.8$ V, $V_{in2} = 1.1$ V and $V_{in3} = 1.3$ V, with $V_{DD} = 3$ V and $V_{TP} = -0.9$ V. When ϕ_1 becomes low, all three node voltages begin to increase, but only V_{o1} stays below V_{DD} , while V_{o2} and V_{o3} are charged to V_{DD} . Those voltage differences are further enlarged when ϕ_2 becomes high. V_{o1} is pulled down to ground, while V_{o2} and V_{o3} stay near V_{DD} (~ 2.65 V). To make sure the circuit functions correctly, the input voltage should not exceed $V_{DD} - |V_{TP}|$ in order to turn all pMOS transistors on during ϕ_1 .

Conclusions: We have reported a simple but efficient min-net circuit capable of selecting the minimum voltage value among its input nodes. It can be implemented in a standard CMOS process, requires small silicon area and consumes low power.

The resolution of the circuit depends mainly on the mismatch among pMOS transistors. The mismatch of transistor size affects the transistor conducting current and parasitic capacitance ($I \propto W/L$ and $C_{1,2,3} \propto WL$). Also the mismatch of transistor gate dioxide thickness affects the transistor threshold voltages and gate capacitance. With 10% variation in threshold voltage V_{TP} and 5% variation of pMOS transistor width W , Monte Carlo simulation shows that the minimum voltage difference among the inputs which the WTA can differentiate is 20 mV.

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CONVOLUTED RAISED-COSINE AND TRIANGULAR-COSINE (RCTC) MODULATION AND ITS PERFORMANCE AGAINST TIMING JITTER OVER NOISY CHANNELS

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Indexing terms: Modulation, Mobile radio systems

The performance of proposed convoluted raised-cosine and triangular-cosine (RCTC) modulation in the presence of Gaussian noise and receiver timing jitter is analysed. The result shows that the new modulation offers a superior BER performance over reported QORC modulation.

Quadrature-overlapped raised-cosine (QORC) modulation is considered more bandwidth-efficient than QPSK and MSK due mainly to its pulse shaping waveform and pulse overlapping before quadrature modulation. With the same transmission rate, the pulse duration in quadrature-overlapped modulation can be twice as wide as that for QPSK or MSK [1, 2]. In QORC modulation, there should be no intersymbol interference due to sampling if sampling to received signal can be perfectly synchronised at $t = 2nT$, where n is any integer, T the bit duration and raised-cosine pulse is defined over $(0, 4T)$ [2]. However, when timing for sampling is jittered because of either nonperfect bit synchronisation, or carrier phase tracking problems or other interference, the sampling from adjacent bits will degrade the bit error rate (BER) performance. Therefore, the shape of the pulse shaping waveform for quadrature-overlapped modulation plays an important role in BER when timing jitter is present. The proposed RCTC pulse shaping waveform is given as follows:

$$p(t) = \begin{cases} -\frac{T \cos(2\pi t/T)}{24\pi^2} + \frac{2T \cos(\pi t/T)}{3\pi^2} + \frac{5T}{8\pi^2} + \frac{t^2}{4T} & (0 < t < T) \\ \frac{T \cos(2\pi t/T)}{24\pi^2} + \frac{2T \cos(\pi t/T)}{\pi^2} + \frac{5T}{8\pi^2} + 4T + \frac{t^2}{4T} + t & (T < t < 3T) \\ -\frac{T \cos(2\pi t/T)}{24\pi^2} + \frac{2T \cos(\pi t/T)}{3\pi^2} - \frac{5T}{8\pi^2} + 4T + \frac{t^2}{4T} - 2t & (3T < t < 4T) \end{cases} \quad (1)$$

which can be normalised by factor $8T/3\pi^2 + T/2$. The edges of the pulse (when either $t = 0$ or $4T$) are flatter than those of the raised-cosine pulse, thus a lower sampling interference level is expected when timing jitter exists. To concentrate on BER for QORC and RCTC modulation with timing jitter, intersymbol interference (ISI) due to limited bandwidth is not considered here. The transmitted signal can be written as

$$s(t) = I(t) \cos \omega t + Q(t) \sin \omega t \quad (2)$$

where $I(t) = A \sum_{n=-\infty}^{\infty} a_n p(t - 2nT)$ and $Q(t) = A \sum_{n=-\infty}^{\infty} b_n p(t - 2nT - T)$ are baseband signals in the I and Q channels, respectively, a_n and b_n take either 1 or -1 , A is the signal amplitude and $p(t)$ is the pulse shaping waveform within $(0, 4T)$. After corruption by Gaussian noise $n(t) = n_c \cos \omega t - n_s \sin \omega t$ with zero mean and variance σ^2 and coherent demodu-

lation, the recovered signal becomes $y_f(t) = I(t) + n_c$ in the I channel. Because the I and Q channels are symmetrical, we need only consider $y_f(t)$ at $(0, 4T)$ when the sampling time is $2T \pm \Delta t$ where Δt represents the timing jitter.

$$y_f(2T \pm \Delta t) = I(2T \pm \Delta t) + n_c \quad (3)$$

where

$$I(2T \pm \Delta t) = A[a_{-1}p(4T \pm \Delta t) + a_0p(2T \pm t) + a_1p(\pm \Delta t)] \quad (4)$$

Without losing generality, we take the positive sign in eqn. 3, thus $p(4T + \Delta t) = 0$ and $p(\Delta t) \neq 0$. Therefore eqn. 3 can be rewritten as

$$y_f(2T + \Delta t) = A[a_0p(2T + \Delta t) + a_1p(\Delta t)] + n_c \quad (5)$$

It can be shown that the average power for a signal given by eqn. 1 is $P_{av} = 2A^2\mu$, where μ is the power of a single pulse $\mu = 1/4T \int_0^{4T} p^2(t) dt$. The signal to noise ratio is $r = 2A^2\mu/\sigma^2$. After calculating the statistical average over a_0 and a_1 in eqn. 5, the BER can be shown to be

$$P_e = \frac{1}{4} \operatorname{erfc} \left\{ \frac{1}{2} \sqrt{\left(\frac{r}{\mu}\right)} [p(2T + \Delta t) + p(\Delta t)] \right\} + \frac{1}{4} \operatorname{erfc} \left\{ \frac{1}{2} \sqrt{\left(\frac{r}{\mu}\right)} [p(2T + \Delta t) - p(\Delta t)] \right\} \quad (6)$$

where $\operatorname{erfc}(x)$ is the complementary error function for x . The BERs for QORC and RCTC modulation with $\Delta t = 0.01T, 0.25T$ and $0.5T$ are plotted in Fig. 1. Fig. 2 shows BER against timing jitter Δt for both modulations with r as a parameter. From Fig. 1, it is seen that RCTC outperforms QORC in BER for different Δt with the SNR gain ranging

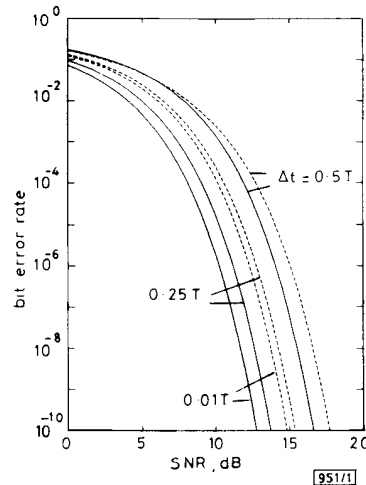


Fig. 1 BER for QORC and RCTC modulation

— RCTC
- - - QORC

from 1.5 dB for $\Delta t = 0.5T$ to 2.2 dB for $\Delta t = 0.01T$, for $P_e = 10^{-6}$. Fig. 2 shows four pairs of curves for $r = 0, 5, 10$ and 15 dB, respectively. When r is large, the performance gap between the two modulation types also becomes large. However, if Δt becomes very large, such as $0.5T$, the BER for different signals deteriorates rapidly and the BER gap tends to shrink.

Conclusions: RCTC modulation performs very well in noisy channels with timing jitter at the receiver. The tolerance of RCTC modulation to timing jitter makes it an ideal modulation scheme for some hostile environments, such as severe