

Low-Voltage Class *AB* Buffers with Quiescent Current Control

Fan You, S. H. K. Embabi, and Edgar Sánchez-Sinencio

Abstract—This paper presents a simple class *AB* buffer which is suitable for low-voltage (1.5 V) applications. The proposed buffer uses an adaptive load to reduce the sensitivity of the quiescent current to the process variation. The main feature of this scheme is its simplicity. The circuit was fabricated in a 2.0 μm digital CMOS process. Experimental results demonstrate that the buffer can operate with a supply voltage below 2 V, and it has the capability to drive small resistive loads.

Index Terms—Class *AB* buffer, low-voltage, quiescent current.

I. INTRODUCTION

A typical op amp consists of a differential input stage, intermediate gain stage, and a class *AB* output stage. Class *AB* buffers are used for their relatively high power conversion efficiency and for their current-handling capabilities which allow them to drive small resistive loads. Under idle conditions, the quiescent current (I_Q) must be as small as possible to reduce the standby power consumption, while the current in the class *B* mode should be as large as possible. In a conventional 5 V op amp, source followers are widely used as class *AB* buffers because of their low output impedance. They are, however, not suitable for low-voltage applications because of their small output swing.

One of the most commonly used low-voltage output buffers was proposed by Monticelli [1]. Modified versions of Monticelli's circuits have been reported in [2], [3]. These circuits were, however, developed for supply voltages ≥ 3 V. A simple circuit without feedback control, which could operate at 1.5 V power supply, was proposed by Pernici *et al.* [4]. In this circuit, the gains of pushing and pulling are different. Therefore, the area of the nMOS output transistor must be increased to compensate for the gain unbalance. It will thus be an inefficient implementation in terms of area. In addition, it requires a complex compensation scheme. The circuit proposed in [5] is another version of a 1.5 V buffer. It also employs a complex compensation scheme, which requires the precise placement of a pole-zero doublet. In addition, the circuit implementation relies on the use of a resistor. Some other interesting buffers have been reported in [6]–[9]. These usually use complex feedback circuits to control the quiescent current.

In this paper, a new 1.5 V class *AB* buffer is proposed. It utilizes a simple adaptive load scheme, instead of a current feedback control, to achieve stable quiescent current [10]. The absence of a feedback loop makes it easier to compensate the op amp to achieve stability. The buffer can operate with a 1.5 V power supply, and is able to drive small resistive loads (100 Ω). The principle and implementation of the proposed buffer

will be described in Section II. Experimental results will be presented in Section III.

II. CLASS *AB* STAGE WITH ADAPTIVE LOAD

A. Principle and Implementation of the Adaptive Load

Fig. 1(a) depicts a class *AB* topology whose quiescent current is not sensitive to process variation. This is due to the reduced gain of the intermediate inverting amplifier stages M_1 and M_2 , which are loaded by the diode-connected transistors M_3 and M_4 , respectively. The gain reduction, however, weakens the drive required for M_p and M_n in the class *B* mode of operation (the gate-to-source voltage swing of M_n and M_p is limited). As a result, the transconductance of M_p and M_n is reduced. To solve this problem, we propose the use of an adaptive load connected to nodes *A* and *B*. Under quiescent conditions, the load will be small to make the quiescent current less sensitive to process mismatch. In the class *B* mode, when the input voltage increases, the resistance connected to node *A* increases, allowing the voltage swing at node *A* to be large enough to provide the maximum drive for the output pMOS transistor (M_p). Similarly, when the input voltage decreases, the resistance at node *B* increases, which enhances the voltage swing at that node.

The proposed output buffer, shown in Fig. 1(b), uses M_6/M_8 and M_5/M_7 as adaptive loads. Under quiescent conditions, M_5 (M_6) is in the saturation region and so is M_7 (M_8). This causes the loading at nodes *B* (*A*) to be small. In the class *B* mode of operation, the gate of M_8 (M_7) is pulled up (down), while its drain voltage drops (increases) because of the presence of M_6 (M_5). This forces M_8 (M_7) out of saturation, and causes the overall resistance of the adaptive load to increase. This is illustrated by the I - V characteristics of both diode-connected load structures shown in Fig. 2. When the buffer operates at the quiescent point, the loads should be biased to operate in the region where their conductance is large. This is determined by the amount of current injected in the loads, e.g., between 1 and 3 μA in the example of Fig. 2. Under these conditions, the quiescent output current in M_n and M_p (I_{oQ}) is not too sensitive to process variations. Outside the 1–3 μA range, the load resistance starts to increase gradually to become significantly large.

At the quiescent point, the two diode-connected loads together with the output transistors can be viewed as two current mirrors. For instance, M_6 , M_8 , and M_n make up a current mirror with β current gain [see Fig. 1(b)]. To ensure that the conductance of the loads M_6/M_8 or M_5/M_7 is small enough when the buffer operates at the quiescent point, M_6 and M_8 (M_5 and M_7) must operate in the saturation region. This can be achieved by selecting V_{b2} and V_{b1} to be equal to $V_{ss} + V_T + 2V_{DS_{\text{sat}}}$ and $V_{dd} - V_T - 2V_{DS_{\text{sat}}}$, respectively, where $V_{DS_{\text{sat}}}$

Manuscript received July 2, 1996; revised October 27, 1997.

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Publisher Item Identifier S 0018-9200(98)03578-1.

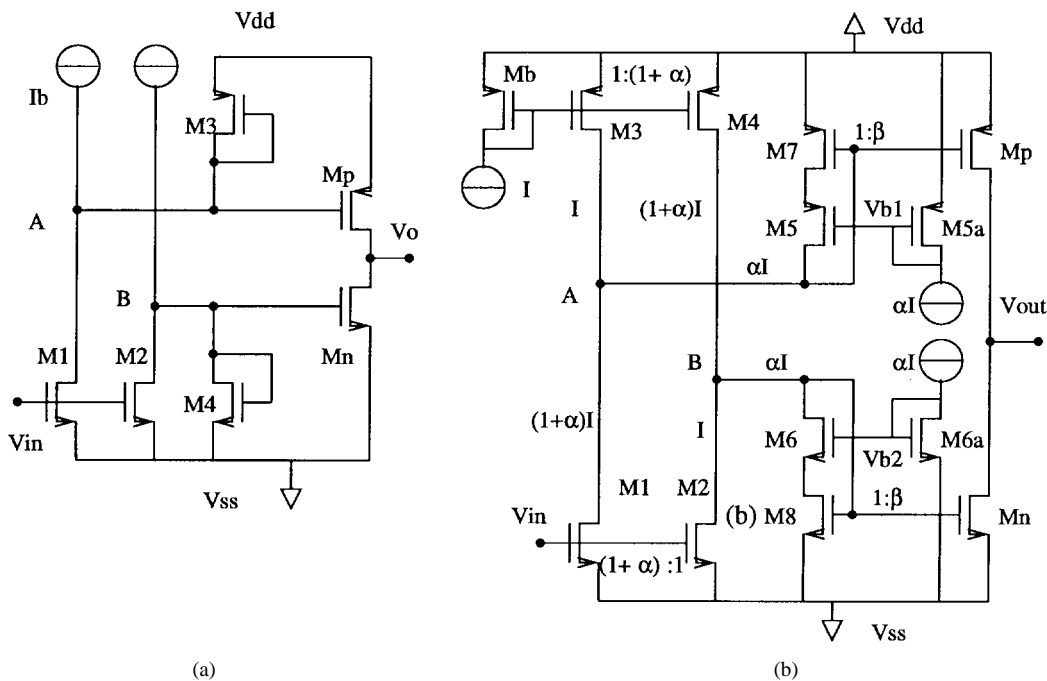


Fig. 1. (a) Output buffer using diode-connected transistors to control quiescent current and (b) output buffer with adaptive load.

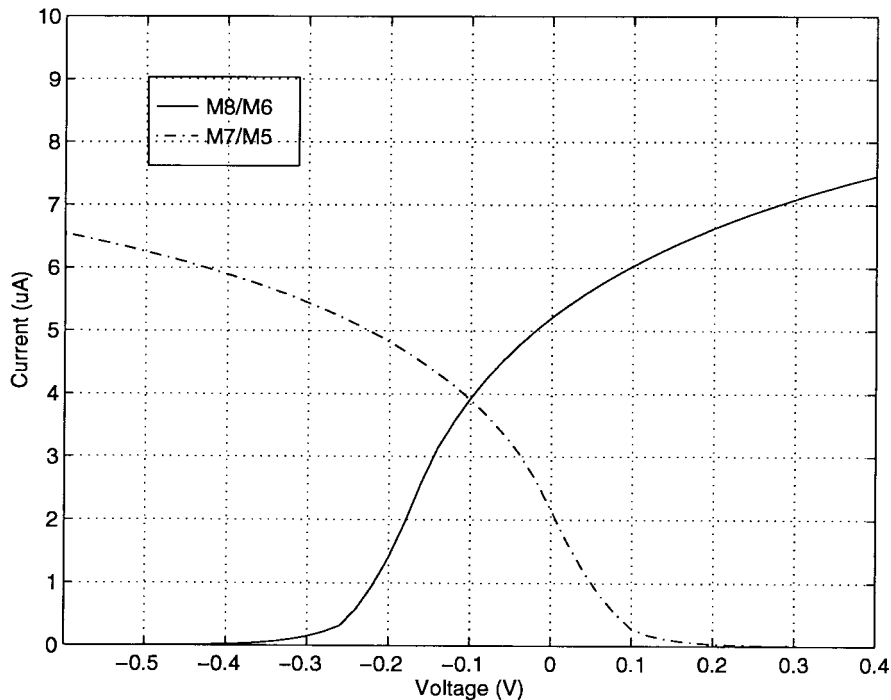


Fig. 2. Simulated I - V characteristics of the adaptive loads in Fig. 1(b) (X axis is V_{in}).

is the saturation drain-source voltage for all four transistors M_5 - M_8 . The biasing scheme proposed for the generalized cascode circuits [11] could be used to generate V_{b1} and V_{b2} as shown in Fig. 1(b). The biasing currents αI for M_{5a} and M_{6a} can be generated by a bandgap reference circuit. The biasing current for M_6/M_8 or M_5/M_7 is a fraction of the biasing current required for the gain stages M_1/M_3 and M_2/M_4 . If the current of the gain stages is I , the current for the loads is αI [see Fig. 1(b)], where $\alpha < 1$. The choice of the value of α will be discussed later. The αI biasing current needed for the

adaptive loads is provided by making the sizes of M_4 and M_1 larger than those of M_3 and M_2 , respectively, by the factor α . The effect of transistor mismatch on the quiescent current of the proposed buffer was analyzed using HSPICE simulations. An op amp configured as a unity-gain follower was used for the simulations. The op amp was constructed by adding an ideal op-amp input stage, with 100 dB gain, in front of the proposed output buffer. A 5 mV mismatch between the threshold voltages of M_3 and M_4 , in the output buffer [see Fig. 1(b)], was introduced. The input (V_{in}) of the unity-gain follower was

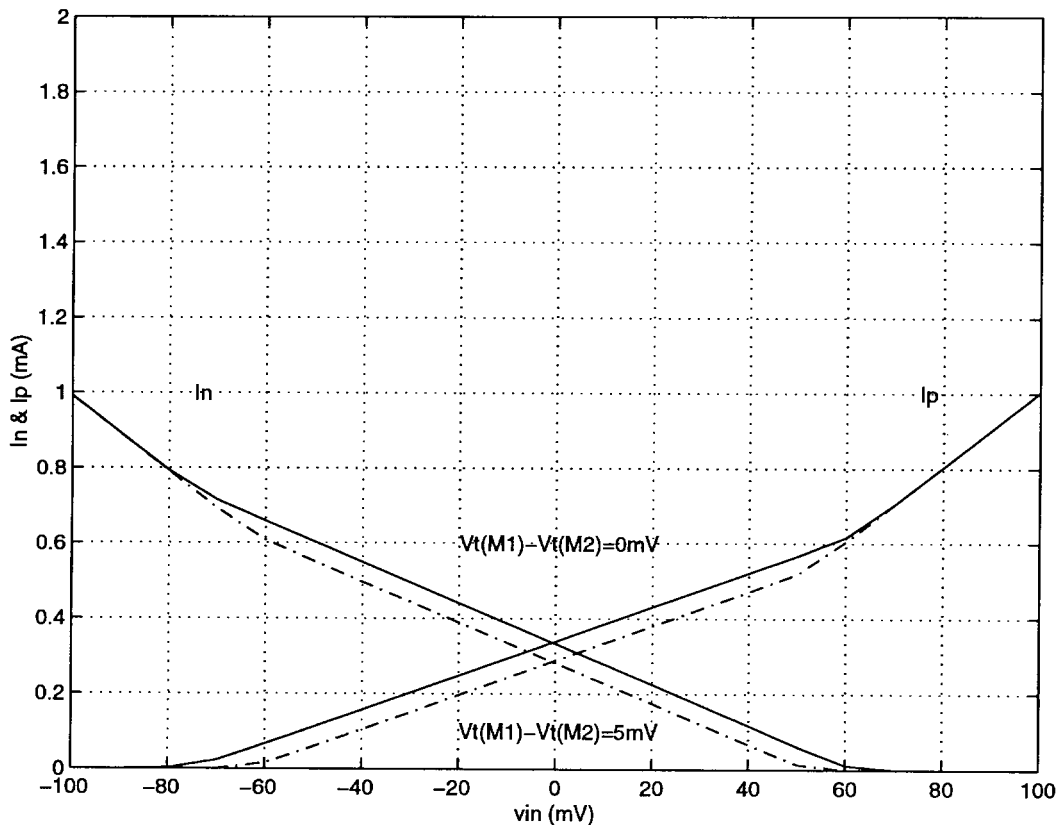


Fig. 3. Simulated variation of the quiescent current with and without 5 mV V_T mismatch.

swept from -100 to 100 mV. Fig. 3 depicts the simulated drain currents of M_p and M_n . The dashed curve shows the current in the presence of 5 mV V_T mismatch. Also shown in the figure is the solid curve which represents the current waveform when there is no mismatch. A comparison of the current values at $V_{in} = 0$ V for both cases indicates that the change of the quiescent current due to the V_T mismatch is relatively small (18%). If no adaptive loads are connected to nodes A and B [see Fig. 1(b)], the quiescent current would change by 460% for a 5 mV V_T mismatch. This demonstrates the effectiveness of the adaptive load in controlling the quiescent current.

The most important feature of the proposed buffer is its capability of achieving fairly good control over the quiescent current without sacrificing the current drive in the class B mode, and with very little area overhead. Its simplicity distinguishes it from other proposed class AB circuits. Another advantage of the proposed buffer is that it can operate with low supply voltage. The required minimum supply voltage is $V_T + 2V_{D_{S_{sat}}}$, which is close to 1.2 V (assuming a $V_{D_{S_{sat}}}$ of 0.2 V, which is feasible in a typical digital CMOS process with a V_T of 0.8 V). In contrast, the class AB buffer in [1] requires at least a $2V_T + 2V_{D_{S_{sat}}}$ supply voltage.

The parameter α in the figure has a significant impact on both the sensitivity of I_{oQ} and the distortion of the buffer. If α is reduced, the conductance of the adaptive load decreases, and the gain of the intermediate stages (M_1/M_3 and M_2/M_4) would increase. This causes I_{oQ} to be more sensitive to process variations. Increasing α would reduce this sensitivity, but has negative implications as far as the distortion

is concerned. This can be explained by considering the THD of a unity-gain follower, which consists of an ideal op amp followed by the proposed class AB buffer. For large α values, the gain of the intermediate gain stages drops, which causes the overall open-loop gain of the op amp to decrease. As a result, the linearity of the closed-loop unity-gain follower is degraded. Fig. 4 depicts simulation results which show how the voltage gain between the input and node A drops as α increases and how the THD of the unity-gain follower suffers as α increases. On the other hand, the sensitivity of the quiescent current, assuming a V_T mismatch of 9 mV, improves as α increases. It is evident that there is a trade off between the sensitivity of the quiescent current and the distortion. A reasonable range for α seems to be anywhere from 0.15 to 0.25.

B. A Three-Stage Amplifier Using the Proposed Buffers

To test the performance and functionality of the proposed class AB buffer, it was incorporated in a three-stage op amp as shown in Fig. 5. The op amp consists of a differential input stage, a noninverting intermediate gain stage, and the proposed class AB buffer. Compensation capacitors C_{m1} , C_{m2} , and C_{m3} are used to stabilize the amplifier, as in the nested Miller compensation topologies [12].

III. EXPERIMENTAL RESULTS

The realization of the class AB buffer based on the concept of adaptive load [Fig. 1(b)] has been fabricated in a $2.0 \mu\text{m}$ n-well digital CMOS process. Fig. 6 shows the measured class AB output current. The aspect ratio of the output nMOS

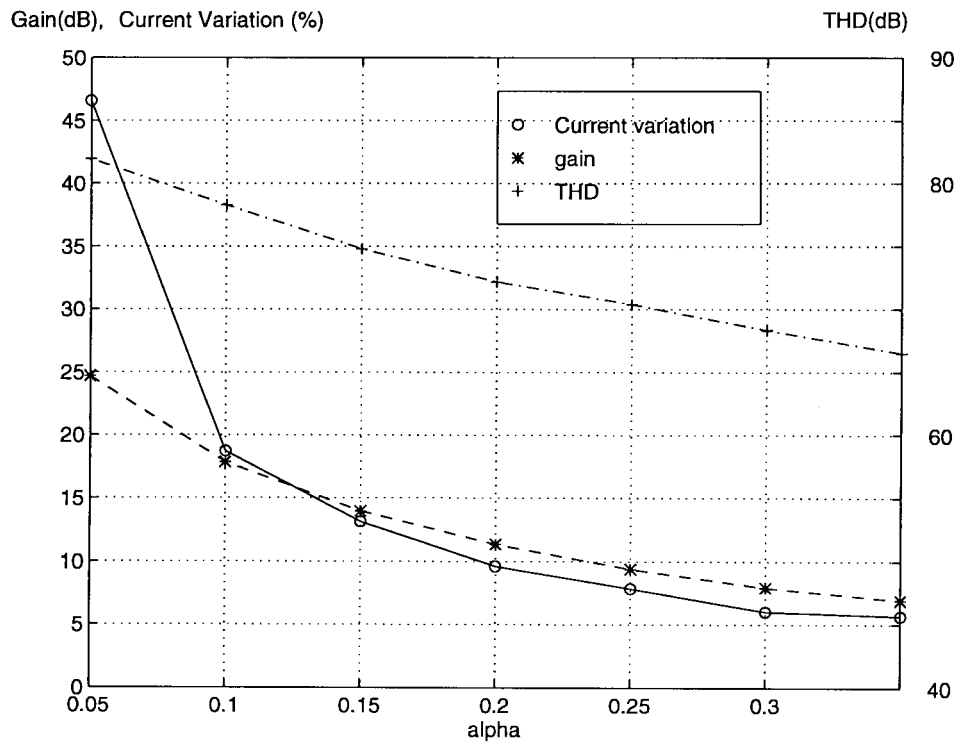


Fig. 4. Simulated quiescent current, voltage gain at node A, and the THD as a function of α .

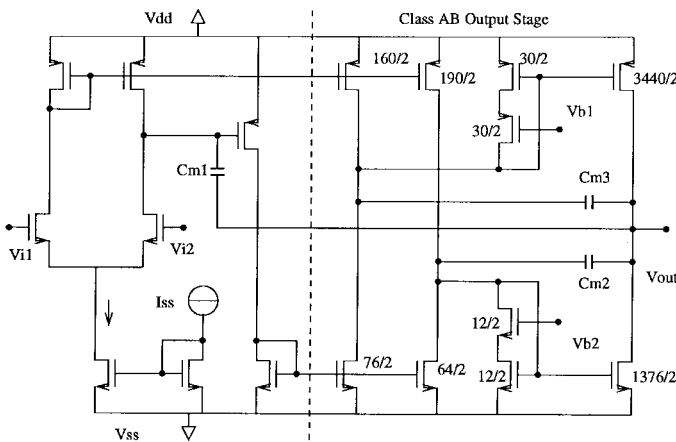


Fig. 5. Schematics of the low-voltage op amp used to test the output buffers.

(M_n) is 1000/3 and that of the pMOS (M_p) is 2500/3. The parameters K'_n and K'_p are 48.8 and 17.0 $\mu\text{A}/\text{V}^2$, respectively. The quiescent current is 295 μA . The ratio between the maximum (class B) current and the quiescent current is about 25. The quiescent current of the four chips received from MOSIS are measured at 220, 270, 295, and 305 μA , respectively. For these four samples, the mean value of the quiescent current is 272 μA and the worst case variation is -19%. For a process with tighter control, the deviation of the quiescent current would be smaller. It is important to note that the measured changes of the quiescent current have an insignificant impact on the op-amp performance such as the gain-bandwidth or phase margin, etc.

The op amp (of Fig. 5) was configured as a unity-gain follower, and was loaded with a 200 Ω resistor in parallel with a 100 pF capacitor. Fig. 7 shows the measured output voltage

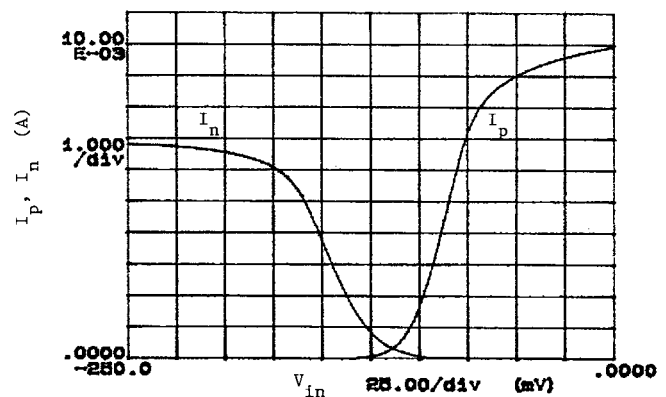


Fig. 6. Measured output current of the class AB output buffer.

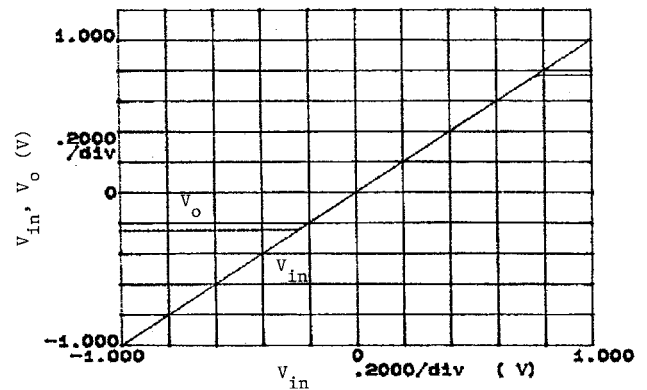


Fig. 7. Measured output voltage versus input voltage of the unity-gain follower.

when the input voltage is swept from V_{ss} to V_{dd} . Fig. 7 shows that the output does not track the input at low levels of V_{in} .

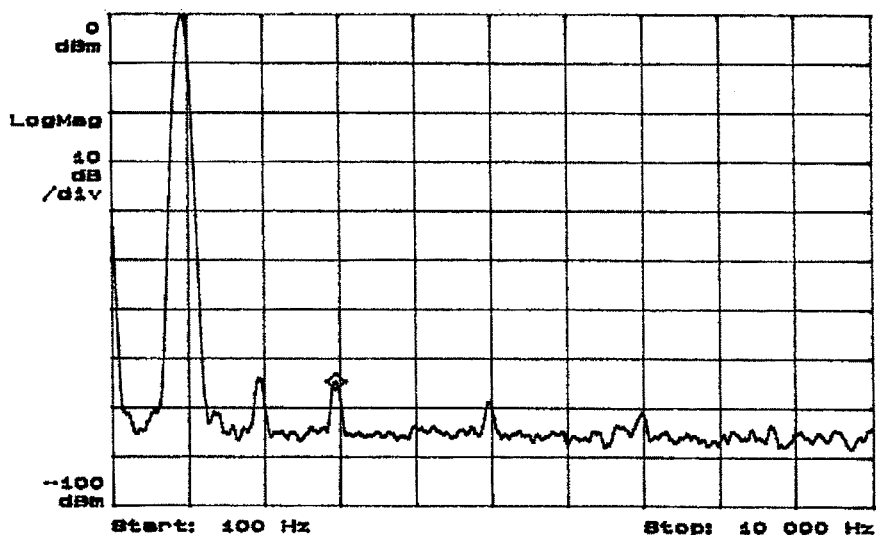


Fig. 8. Magnitude spectrum at the output node of a unity-gain follower with 1 kHz sine wave input.

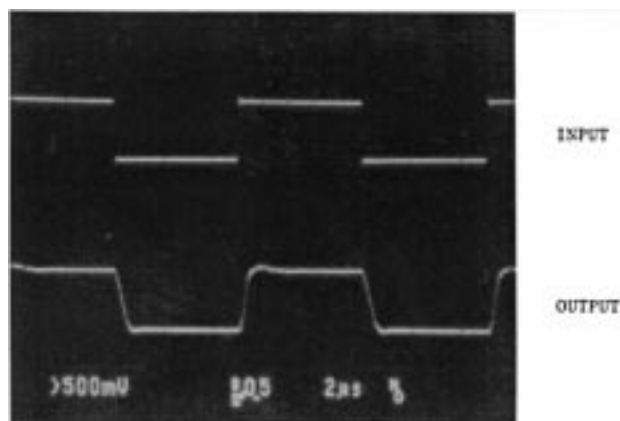


Fig. 9. Measured 0.8 V/100 kHz step response of three-stage op amp with proposed buffer.

This is not due to any limitations imposed by the output buffer, but rather is due to the limited common-mode range (CMR) of the differential input stage. The input differential stage turns off when the input voltage falls below the lower bound of the CMR. The lower bound of the CMR is determined by the threshold voltage of the input transistors of the differential pair. In the process used for fabrication, $V_T = 0.86$ V. This explains why the output deviates from the input when V_{in} approaches the lower rail (see Fig. 7). Better tracking can be achieved by reducing the lower bound of the CMR, which can be, in turn, achieved by using low V_T input transistors or by floating-gate transistors [13]. The output node of the unity-gain follower was measured at 72 dB of THD when a 1 kHz 0.8 V p-p sine wave is applied at the input. Fig. 8 shows that the harmonic with the highest magnitude is 74 dB below the fundamental at 1 kHz. A 0.8 V step input has been applied to the unity-gain follower. No oscillations were observed in the step response, as illustrated in Fig. 9, which implies that the amplifier is stable. Since the common-mode range of the input stage (differential pair) is between

$V_{ss} + 1.0$ V and V_{dd} , we used a 2 V supply voltage to achieve a 1 V swing.

IV. CONCLUSION

A circuit technique to control the quiescent current of low-voltage class AB buffers has been proposed. This simple class AB buffer achieves good quiescent current control by using an adaptive load. Experimental results verify the operation of the proposed buffer, and demonstrate that the quiescent current can be controlled with reasonable precision. The experiments also show that an op amp using the proposed buffers can be easily stabilized.

ACKNOWLEDGMENT

The authors would like to thank A. Ganesan for the discussion on the problems associated with the quiescent current control in low-voltage class AB buffers.

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