

Constant- g_m Rail-to-Rail CMOS Op-Amp Input Stage with Overlapped Transition Regions

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Abstract—Conventional techniques to achieve a constant- g_m rail-to-rail complementary N-P differential input stage require complex additional circuitry. In addition, the frequency response and common-mode rejection ratio (CMRR) are degraded. An economical but efficient design technique to overcome these problems is proposed. The proposed technique strategically overlaps the transition regions of the tail currents for the n- and p-pairs to achieve constant overall transconductance. Experimental results demonstrate that g_m variation can be restricted to within $\pm 4\%$ with improved CMRR and frequency response.

Index Terms—Amplifiers, low-voltage circuits, nonlinear circuits.

I. INTRODUCTION

THE NEED for analog circuits that can operate with low power-supply voltage has increased in recent years. The lowering of the supply voltage results in a reduced input common-mode range. An op-amp can easily be designed to achieve rail-to-rail output swing with simple class-A or class-AB designs. The key problems lie at the input stage, and the classic two-stage architecture demands a rail-to-rail transconductor function with both constant g_m and limiting current, so that unity-gain bandwidth and slew rate are both maintained over the full common-mode input range. Rail-to-rail input stages allow input common-mode signals to vary from the negative to positive supply rails by the use of complementary differential pairs operated in parallel. When the common-mode input signal is near one of the rails, only one of the pairs turns on; the other is cut off. At the middle of the common-mode input range, both the n- and p-pairs are on, and the total transconductance has twice the g_m of a single pair, assuming both pairs have the same g_m value. Because of this, the total transconductance is not constant across the input common-mode range. This is an undesired phenomenon because it not only results in nonconstant gain and variable unity-gain frequency but also degrades the common-mode rejection ratio (CMRR) and causes the slew rate to vary.

A number of techniques to achieve constant g_m has been proposed [1]–[10]. Stabilization of the total g_m over the common-mode range can be tackled by varying the effective tail current in the active differential pair, so that its g_m doubles when the other is inactive. A simple way to achieve this is to use a transistor to sense that one of the pairs has lost sufficient gate drive to operate and to divert the unused tail current through a bypass transistor [1]–[4]. An alternative technique is to increase the tail current bias on each side by a factor of four and to add additional devices inside each differential pair, which have a width three times that of the active devices. If the square-law operation is valid, g_m will double, making up the deficit caused by the inactive pair [10]. In these implementations, the diverting transistor is three times wider than the driving transistor, which causes extra tail current added to the large signal limiting value. Hence slewing value doubles within the common input range. To remedy this, a novel implementation that employs a diverting transistor of the same size as that of the driving transistor has been recently reported [12]. Different from the techniques handling the dc tail current, a method based on processing signal current has been proposed [11]. There, the signal currents from the n- and p-pairs are compared, and only the maximum current is selected and processed, keeping the g_m constant. All the above techniques need extra circuitry such as many current mirrors [1]–[3]; signal-processing circuits as maximum-selecting circuitry [11], which requires even more mirrors; or four 1:1 mirrors accompanying the current diverting circuit [11]. All these implementations make the input stage much more complicated and inevitably require more chip area and power consumption compared with the conventional input stage. Furthermore, these techniques often have degraded CMRR [15], [16].

In this paper, a novel technique to obtain a constant g_m as well as to achieve rail-to-rail input and output swings are presented. This paper is organized as follows. Section II presents an analysis of the complementary input stage and introduces the idea of overlapping the transition regions of the tail currents for the n- and p-pairs to achieve constant overall transconductance g_m . The proposed complementary input stage using a pair of dc level shifters to overlap the transition regions is presented in Section III. Section IV presents the proposed op-amp with the implementation of dc level shifters in the complementary input stage. Section V shows the simulated and experimental results of the designed op-amp. Section VI provides the conclusions.

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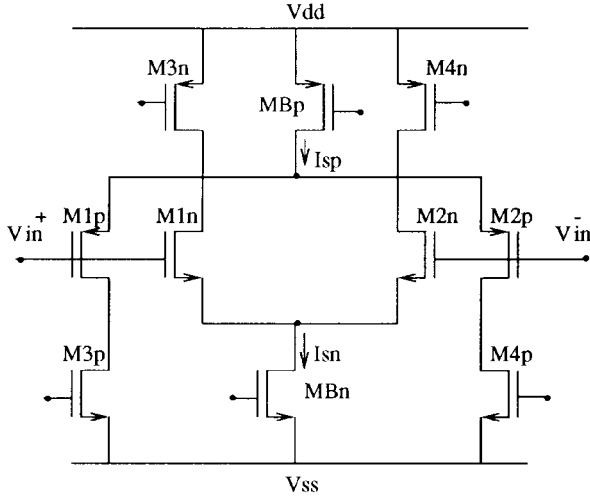


Fig. 1. Schematic of a complementary input stage.

II. ANALYSIS OF COMPLEMENTARY INPUT STAGE

The schematic of a complementary input stage is shown in Fig. 1, where M1n, M2n, and M1p, M2p constitute the n- and p-type differential input pairs, respectively.

The g_m of this input stage is constant if the following equation is satisfied [1], [6]:

$$\sqrt{\beta_n I_{sn}} + \sqrt{\beta_p I_{sp}} = \text{constant} \quad (1)$$

where $\beta_n = \mu_n C_{ox} W_n / L_n$, $\beta_p = \mu_p C_{ox} W_p / L_p$, and I_{sn} and I_{sp} are the bias current for the n- and p-pair transistors, respectively. By choosing $\beta_n = \beta_p$, g_m is constant if $\sqrt{I_{sn}} + \sqrt{I_{sp}}$ is constant.¹ Fig. 2 shows three regions of operation, for I_{sn} and I_{sp} . The current in each region is described as follows:

Cutoff

$$I_{sn} = 0, \quad V_{ss} \leq V_{cm} \leq V_n^- \quad (2)$$

Transition

$$I_{sn} = I_{sn}(V_{cm}), \quad V_n^- < V_{cm} \leq V_n^+ \quad (3)$$

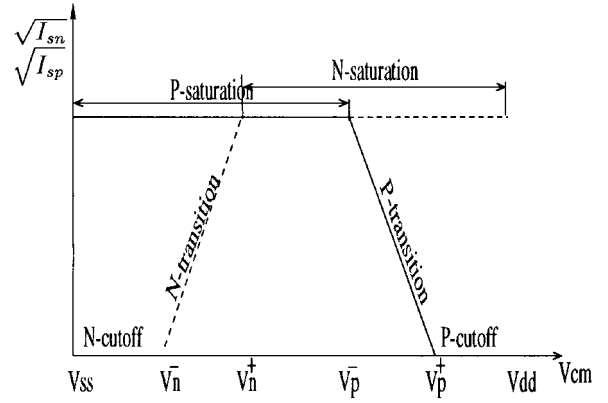
*Saturation*²

$$I_{sn} = I_{sn0} = \frac{\beta_{MBn}}{2} (V_{G_MBn} - V_{ss} - V_{tn})^2, \quad V_n^+ < V_{cm} \leq V_{dd} \quad (4)$$

where I_{sn0} is the saturation current for the n-pair transistors. In the *cutoff* region, M1n and M2n are in cutoff, MBn is in linear region, and the currents through them are all zero. In the *transition* region, M1n and M2n are in saturation, and MBn is in the linear region. The voltage V_{DS_MBn} is very small when V_{cm} approaches V_n^- , and increases with increasing V_{cm} until MBn enters into the saturation region. In the maximum I_{sn} region, as specified by (4), all three transistors (M1n, M2n, and MBn) enter into the saturation region. The subthreshold region

¹The assumption that g_m is proportional to $\sqrt{I_{sn}} + \sqrt{I_{sp}}$ is valid as long as the square-law model of the MOS transistors is valid. The MOS transistors used in this work have channel lengths of at least 1.2 μm . Thus the square-law model can be used. This has been verified through HSPICE simulations using a Berkeley Short-Channel IGFET Model (BSIM).

²*Saturation* here refers to the region where the tail current reaches its final volume. It is not to be confused with the saturation region of a MOS device.

Fig. 2. Illustration of tail current I_{sp} (solid line) and I_{sn} (dashed line) across common-mode input V_{cm} .

between the cutoff and the transition region is not considered here for the sake of simplicity.

The lower boundary of the transition region V_n^- is given by

$$V_n^- = V_{ss} + V_{tn} + V_{DS_MBn}. \quad (5)$$

The fact that I_{D_MBn} is almost zero at V_n^- and that V_{GS_MBn} is always greater than V_{tn} implies that V_{DS_MBn} must be negligible, so (5) can be approximated by

$$V_n^- \approx V_{ss} + V_{tn}. \quad (6)$$

At the upper boundary of the transition region V_n^+ , MBn is at the transition from the linear to the saturation, i.e.,

$$V_{DG_MBn} = -V_{tn}. \quad (7)$$

Since V_{DG_MBn} can be expressed as $V_n^+ - V_{tn} - \sqrt{I_{sn0}/\beta_{M1n}} - V_{G_MBn}$, (7) can be rewritten as

$$V_n^+ = V_{G_MBn} + \sqrt{\frac{I_{sn0}}{\beta_{M1n}}}. \quad (8)$$

To derive a general expression for I_{sn} in the transition region, consider the following equations:

$$I_{sn} = \beta_{M1n} (V_{cm} - V_{D_MBn} - V_{tn})^2 \quad (9)$$

$$I_{sn} = \beta_{MBn} \left(V_{G_MBn} - V_{ss} - V_{tn} - \frac{V_{D_MBn} - V_{ss}}{2} \right) \cdot (V_{D_MBn} - V_{ss}). \quad (10)$$

To simplify the analysis, we assume $(W/L)_{MBn} = 2(W/L)_{M1n}$, i.e.,

$$\beta_{MBn} = 2\beta_{M1n}. \quad (11)$$

V_{D_MBn} can be solved from (9)–(11) to be

$$V_{D_MBn} = \frac{V_{cm} + V_{G_MBn}}{2} - V_{tn} - \frac{1}{2} \sqrt{2(-V_{tn} + V_{G_MBn} - V_{ss})^2 - (V_{cm} - V_{G_MBn})^2}. \quad (12)$$

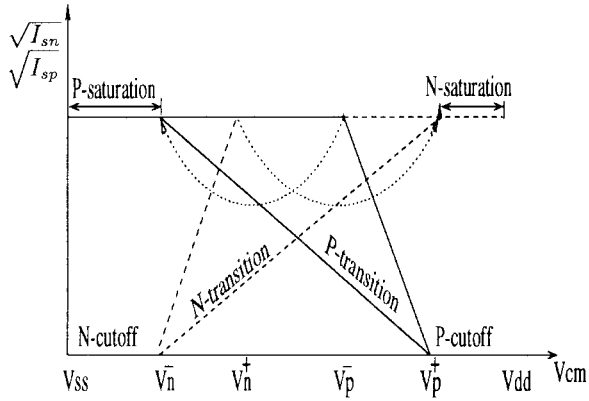


Fig. 3. Overlap transition regions by moving V_p^- left and V_n^+ right [see (17) and (18)].

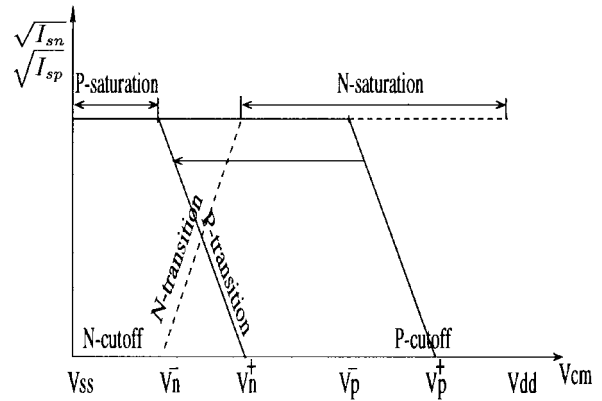


Fig. 5. Overlap transition regions by shifting n-pair curve left.

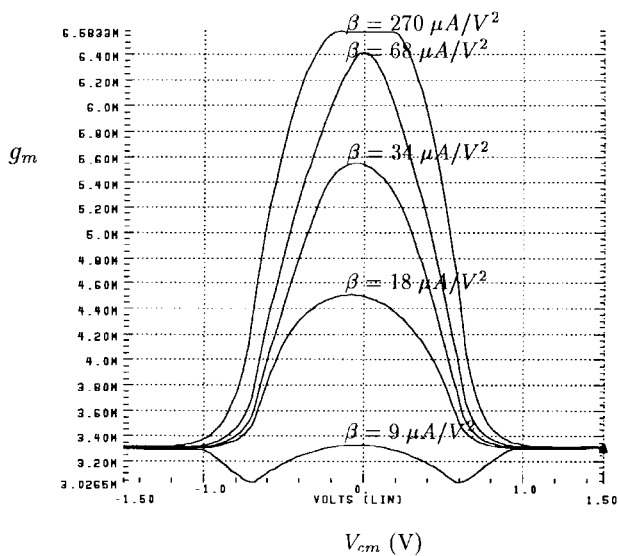


Fig. 4. Plot of g_m versus V_{cm} for different β .

Substituting for V_{D_MBn} from (12) in (9), we have (13), shown at the bottom of the page. It can be verified from (13) that I_{sn} is zero for $V_{cm} = V_n^-$, and it is I_{sn0} for $V_{cm} = V_n^+$.

The boundaries of the transition region for the p-pair can be found similarly to be

$$V_p^+ = V_{dd} + V_{tp} \quad (14)$$

$$V_p^- = V_{G_MBn} - \sqrt{\frac{I_{sp0}}{\beta_{M1p}}} \quad (15)$$

I_{sp} is shown in (16) at the bottom of the page. One can also easily verify from (16) that I_{sp} is zero for $V_{cm} = V_p^+$, and it is I_{sp0} for $V_{cm} = V_p^-$, where I_{sp0} is the current in the saturation region for the p-pair, i.e., $I_{sp0} = (\beta_{MBp}/2)(-V_{G_MBp} + V_{dd} + V_{tp})^2$.

We note that although (13) and (16) are derived under the assumption of (11), this assumption is not necessarily required. With the help of MAPLE, we have observed that as long as β_{MBn} is comparable with β_{M1n} , very similar results to (13) and (16) can be obtained. So we will use these two equations in the following analysis.

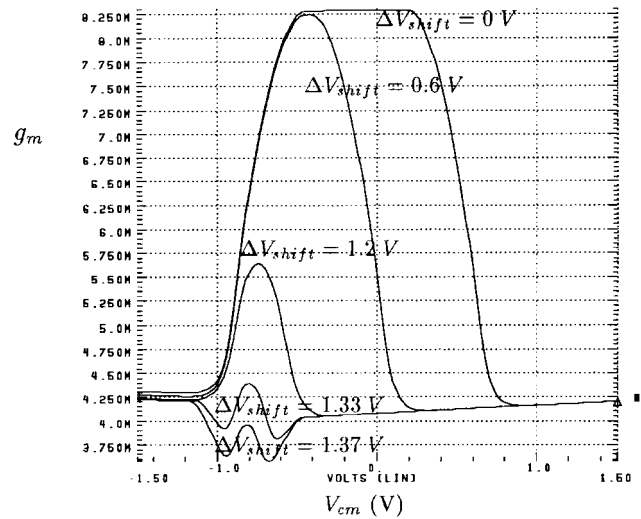


Fig. 6. g_m versus V_{cm} for different V_{shift} .

$$I_{sn} = \beta_{M1n} \left[\frac{V_{cm} - V_{G_MBn}}{2} + \frac{1}{2} \sqrt{2(-V_{tn} + V_{G_MBn} - V_{ss})^2 - (V_{cm} - V_{G_MBn})^2} \right]^2 \quad (13)$$

$$I_{sp} = \beta_{M1p} \left[\frac{-V_{cm} + V_{G_MBp}}{2} + \frac{1}{2} \sqrt{2(V_{tp} - V_{G_MBp} + V_{dd})^2 - (V_{cm} - V_{G_MBp})^2} \right]^2 \quad (16)$$

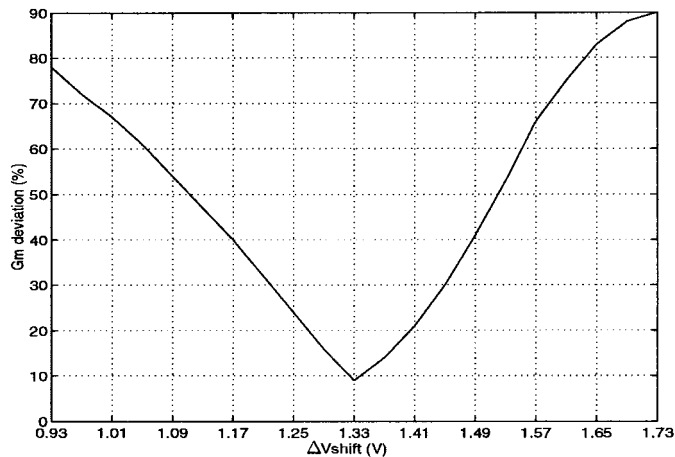


Fig. 7. g_m deviation versus ΔV_{shift} .

Equations (13) and (16) show that $\sqrt{I_{\text{sn}}}$ is monotonically increasing within the transition region while $\sqrt{I_{\text{sp}}}$ is monotonically decreasing. If the transition regions of the n- and p-pairs are properly overlapped, a relatively constant $\sqrt{I_{\text{sn}}} + \sqrt{I_{\text{sp}}}$ or g_m can be achieved.

By the symmetry between the n- and p-pairs, we can assume that $I_{\text{sp}0} = I_{\text{sn}0}$, $\beta_{\text{M1p}} = \beta_{\text{M1n}}$, and $V_{\text{G_MBp}} = -V_{\text{G_MBn}}$. We also assume that $V_{\text{tp}} = -V_{\text{tn}}$ for simplicity. Recall that the boundaries of the transition regions are as expressed by (6), (8), (14), and (15), where V_n^- and V_p^+ are mainly determined by the process parameters such as V_{tn} or V_{tp} while V_n^+ and V_p^- depend on the dimensions of the transistors of the differential pairs. Let

$$V_p^- = V_n^- \quad (17)$$

or, equivalently

$$V_n^+ = V_p^+ \quad (18)$$

which means the transition regions of the n- and p-pairs are overlapped. As illustrated in Fig. 3, we locate V_p^- exactly at the same position as V_n^- , and locate V_n^+ at V_p^+ . Using (8) and (14), we have

$$V_{\text{G_MBn}} + \sqrt{\frac{I_{\text{sn}0}}{\beta_{\text{M1n}}}} = V_{\text{dd}} + V_{\text{tp}}. \quad (19)$$

Therefore

$$\beta_{\text{M1n}} = \frac{I_{\text{sn}0}}{(V_{\text{dd}} + V_{\text{tp}} - V_{\text{G_MBn}})^2} = \beta_{\text{M1p}}. \quad (20)$$

With the β 's determined by (20), the two transition regions would overlap. Given typical values of $I_{\text{sn}0} = 11 \mu\text{A}$, $V_{\text{dd}} = 1.5 \text{ V}$, $V_{\text{tp}} = -0.8 \text{ V}$, and $V_{\text{G_MBn}} = -0.25 \text{ V}$, β_{M1n} is calculated to be $12 \mu\text{A}/\text{V}^2$. Fig. 4 shows the simulated³ g_m versus V_{cm} for different β for a complementary input stage. The most constant g_m is achieved when β is equal to $9 \mu\text{A}/\text{V}^2$,

³The BSIM has been used in HSPICE simulations.

which is close to the theoretical value of $12 \mu\text{A}/\text{V}^2$, verifying our theoretical analysis. The optimal g_m obtained in Fig. 4 is constant within 9%.

Suppose $KP_n = 60 \mu\text{A}/\text{V}^2$, and for the above calculated $\beta = 12 \mu\text{A}/\text{V}^2$, the aspect ratio of M1n is 1/5. Aspect ratios of the input transistors of the differential pairs are calculated to be less than one for n-pair and close to one for p-pair. These small β 's for the input differential pairs widen and linearize the transition regions where the increasing $\sqrt{I_{\text{sn}}}$ and the decreasing $\sqrt{I_{\text{sp}}}$ cancel each other, thus yielding a constant g_m . Unfortunately, the small aspect ratios of the differential pairs degrade the noise performance and cause the circuit to be more sensitive to the mismatch between the pair transistors.

III. COMPLEMENTARY INPUT STAGE WITH DC LEVEL SHIFTER

In this section, we present another technique to overlap the transition regions without sacrificing the g_m . From the analysis carried out in the previous section, we know that as long as the two transition regions overlap properly, constant g_m can be obtained. It can be observed from (13) and (16) that β is proportional to the slopes of the curves for the transition region. To obtain overlapped transition regions while preserving the original slope of the curve (i.e., keeping the original large β) in the transition region, a dc level shifter can be introduced to shift the p-transition curve leftward to overlap the n-transition curve as shown in Fig. 5. If the level shifting is too small, g_m exceeds the nominal constant value. If the amount of level shifting is too large, g_m drops below the nominal constant value. There is an optimal shift $\Delta V_{\text{optimal}}$, which yields a constant g_m . This optimal shift can be easily realized using a conventional source follower.

Since it is difficult to derive an expression for the optimal shift $\Delta V_{\text{optimal}}$, we have used MAPLE to identify narrow range within which the optimal value for ΔV_{shift} exists. This range can be defined as follows:

$$2V_{\text{G_MBn}} < \Delta V_{\text{optimal}} < 2V_{\text{G_MBn}} + \sqrt{\frac{I_{\text{sn}0}}{\beta_{\text{M1}}}}. \quad (21)$$

Fig. 6 shows the simulated value of $\sqrt{I_{\text{sn}}} + \sqrt{I_{\text{sp}}}$ versus V_{cm} for different values of the amount of level shifting ΔV_{shift} . The op-amp used for the simulation to generate the results in Fig. 6 is illustrated in Fig. 8. From Fig. 6, we observe that the optimal $\Delta V_{\text{shift}} \approx 1.33 \text{ V}$, which is between the lower bound $2V_{\text{G_MBn}} = 1.2 \text{ V}$ and the upper bound $V_{\text{G_MBn}} + V_{\text{tn}} + V_{\text{ss}} = 1.37 \text{ V}$, as anticipated by (21). It is noticeable in Fig. 6 that the optimal ΔV_{shift} is closer to the upper bound $V_{\text{G_MBn}} + V_{\text{tn}} + V_{\text{ss}}$. This is because the actual V_n^+ (V_p^-) is smaller (greater) than those shown in (8) [(15)], as long as MBn and MBp operate in the linear region. This means that the two transition regions are further apart from each other than defined by (8) and (15), and thus more shift is needed to overlap the transition regions. The g_m corresponding to the optimal shift is constant within 9%. Fig. 7 shows the deviation of g_m with respect to the ΔV_{shift} ; for ΔV_{shift} varying

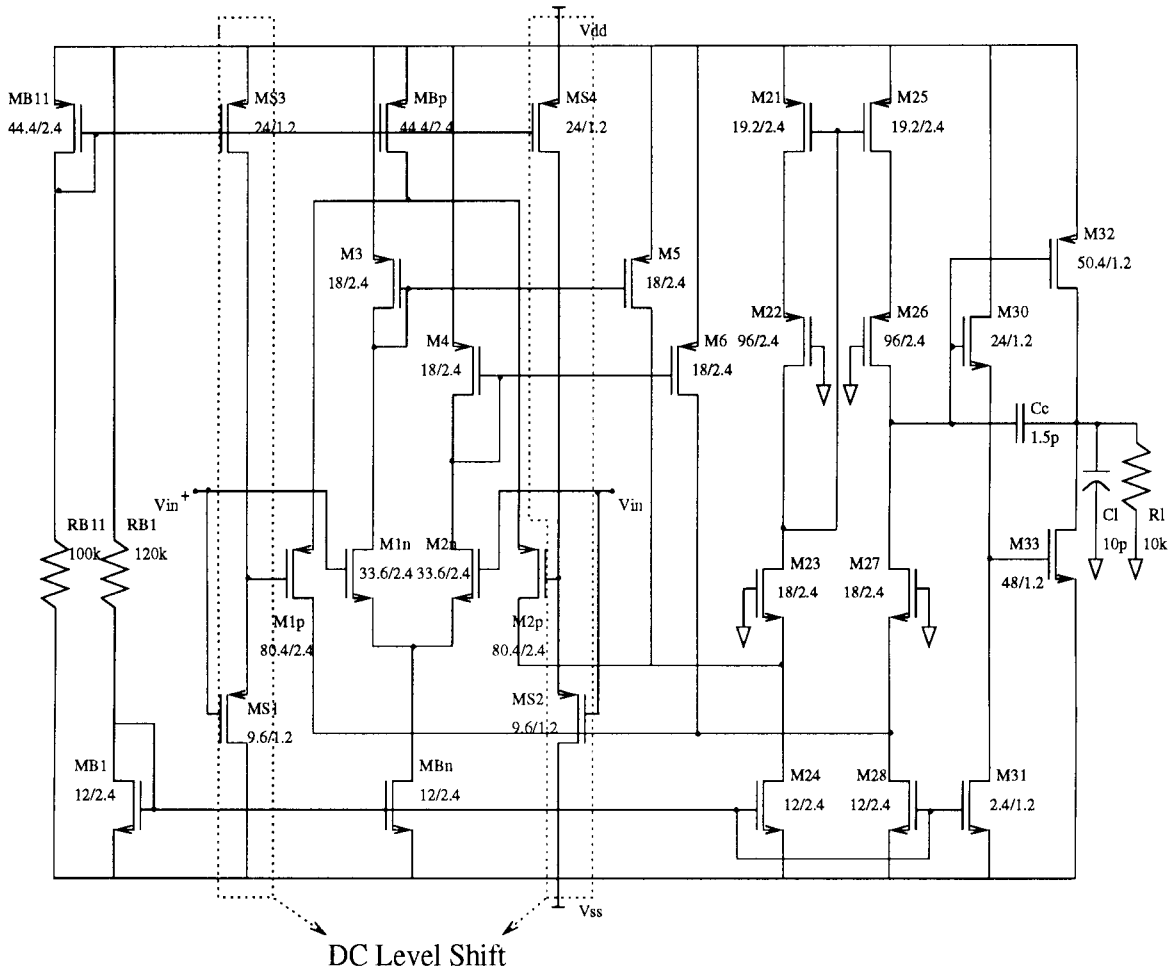


Fig. 8. Schematic of the op-amp with level shifters in the complementary input stage.

by ± 0.4 V, the g_m deviates from its optimal 9% up to about 90%.

IV. IMPLEMENTATION OF AN OP-AMP WITH COMPLEMENTARY INPUT STAGE USING DC LEVEL SHIFTERS

Fig. 8 shows the op-amp with the dc level shifters in the complementary input stage. The pair of dc level shifters is implemented by two pairs of PMOS source followers MS1–MS4, as indicated in Fig. 8. The op-amp consists of three stages: the complementary input stage, the folded cascode stage M21–M28, and the class AB output stage M30–M33. Transistors MB1 and MB11 are used to bias the circuit, and their dimensions also determine V_{G_MBn} and V_{G_MBp} , respectively. The folded cascode stage provides high gain while keeping the input and output swing high. Last, the class AB output stage ensures rail-to-rail output swing. Simplicity is obvious in our design compared with the others, where such circuits as 1 : 3 current mirror [1]–[3], square-root circuit [1], [6], current bleed circuit [7], maximum-selecting circuit [11], and current diverting circuit [12] are used to maintain the near constant g_m .

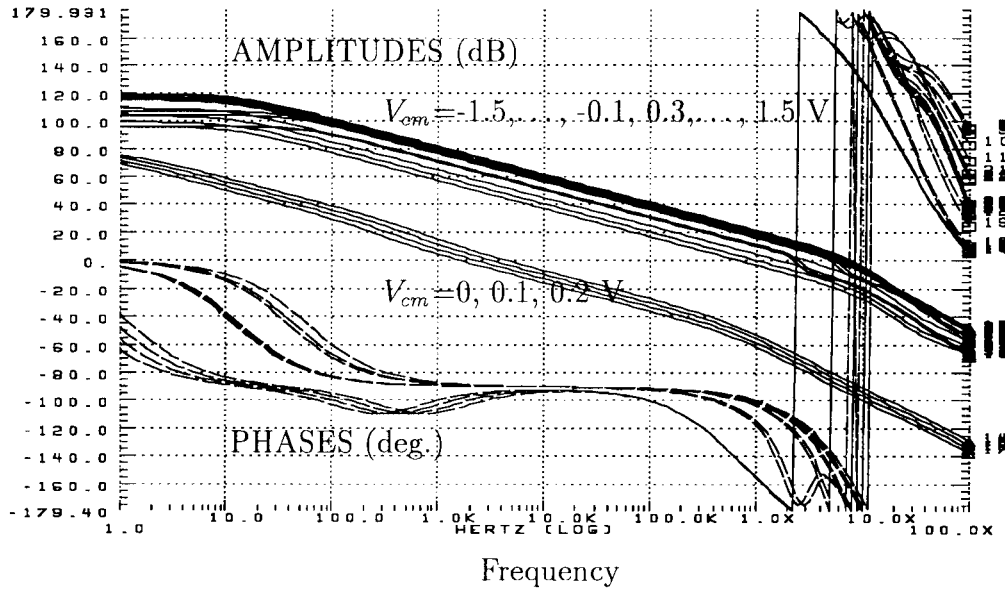
Fig. 9(a) shows the frequency responses of the op-amp with the conventional complementary input stage, as shown in

Fig. 1. The amplitudes and the phases are heavily dependent upon the applied common-mode input voltage V_{cm} , which is varied from rail (-1.5 V) to rail (1.5 V) by a step of 0.1 V. This op-amp is unstable and cannot be compensated due to the varying g_m , as we stated in the introduction. In contrast, Fig. 9(b) shows the frequency responses of the op-amp with level-shifted input stage for the common-mode input voltage V_{cm} varying from rail to rail by a step of 0.1 V. The amplitudes and the phases of the proposed op-amp are almost independent of the applied V_{cm} . Comparing Fig. 9(a) and (b), we can see the substantial improvement in the frequency responses of the proposed op-amp over that of the op-amp of Fig. 1.

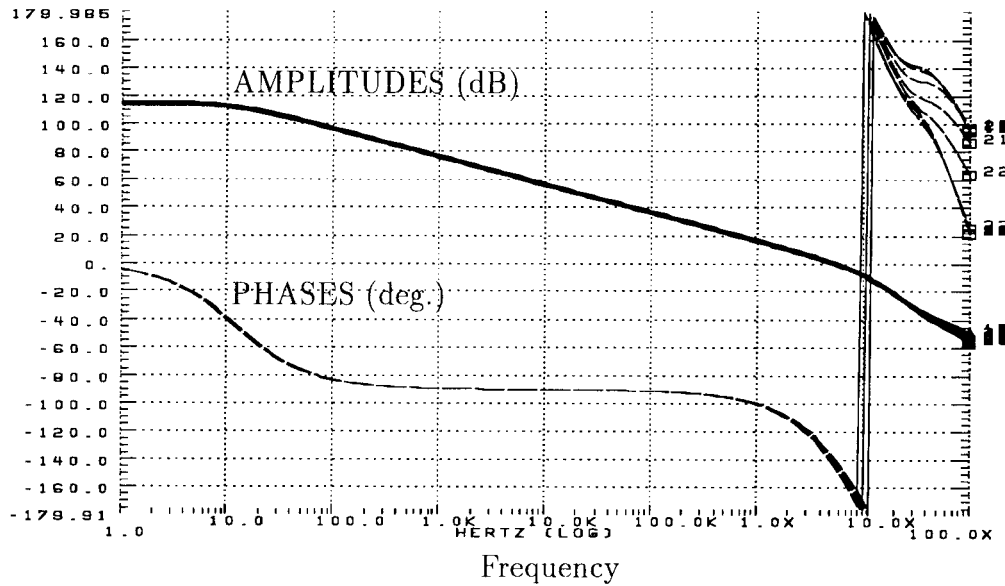
Fig. 10 shows comparison of the CMRR of the conventional complementary input stage and that of the input stage with dc level shifters. It can be observed that by using dc level shifters, the degradation of the CMRR is reduced to 45 dB, compared to 55 dB for the case that uses no level shifters.

V. SIMULATION AND EXPERIMENTAL RESULTS

The simulation results of the op-amps are shown in Table I. Monte Carlo 3σ analysis was carried out to see the deviations of the g_m caused by the deviations of the process parameters V_{TO} and KP. It was simulated for 100 runs for



(a)



(b)

Fig. 9. Frequency responses of op-amps for the input stages (a) without and (b) with level shifters. Common-mode input V_{cm} varies from rail to rail by a step of 0.1 V.

both the input differential pairs and the level shifters with V_{TO} and KP deviation of 5 and 10%, respectively. Table II shows the variations of the g_m for the assumed process deviations.

The g_m is more sensitive to V_{TOP} and KP_P variation because they affect both the dc level shifters and the PMOS input differential pairs.

The op-amp shown in Fig. 8 is fabricated using a 1.2- μm n-well CMOS technology. Fig. 11 shows the microphotograph of a chip with four identical op-amps. The area of each op-amp is 0.12 mm^2 .

Fig. 12 shows the measured input-output transfer characteristic of the op-amp, which is configured as a unity-gain

follower and loaded with a 10-k Ω resistor. The figure shows that the op-amp has a rail-to-rail common-mode input voltage range, as well as a rail-to-rail output voltage swing.

Fig. 13 shows the transconductance g_m , which is obtained from the measurement of $\sqrt{I_{sn}} + \sqrt{I_{sp}}$. As expected from the analysis in Section V the process variation and the layout mismatch cause g_m to deviate from the designed value. The dashed line in Fig. 13 is the measured g_m , which is constant within -13% , although we expect it to be within $\pm 5\%$. More flat g_m can be obtained by tuning the bias resistors RB1 and RB11 in Fig. 8 or, more accurately, by tuning the bias currents I_{sn0} and I_{sp0} . As shown in Fig. 13, by decreasing the bias current of I_{sn0} or I_{sp0} from 15.2 to 13 μA , we decrease the

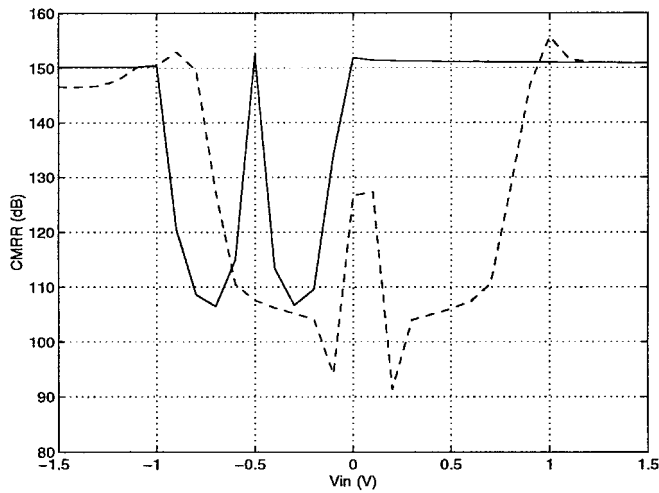


Fig. 10. Comparison between the CMRR of the conventional complementary input stage (dashed line) and that of the input stage with dc level shifters (solid line).

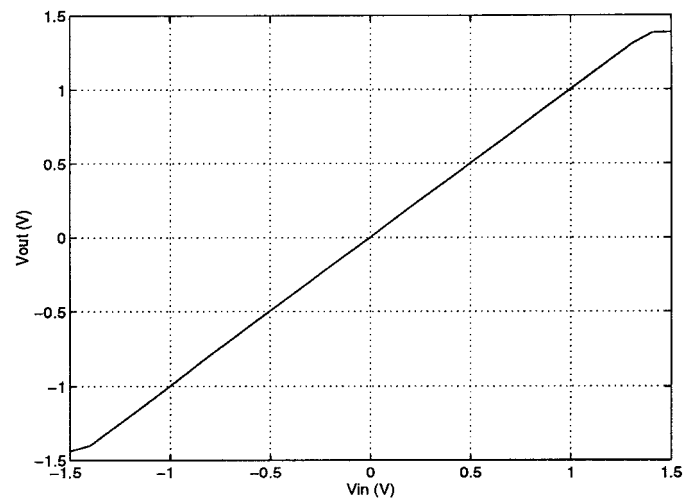


Fig. 12. Measured input-output characteristic.

TABLE I
SIMULATION RESULTS OF THE OP-AMP ($V_{dd} = \pm 1.5$ V)

Parameter	Value
Input offset voltage	-0.5 mV
Common mode input voltage range	-1.42-1.43 V
Output voltage swing	1.46-1.43 V
Voltage Gain	113 dB
GBW	5.5 MHz
Min. CMRR (@DC)	105 dB
Slew rate	12 V/ μ s
Maximum input (1% THD)	1.8 μ V

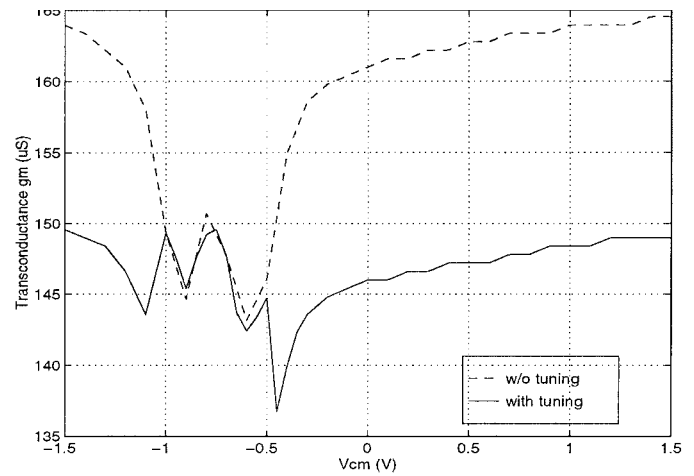


Fig. 13. Measured transconductance g_m .

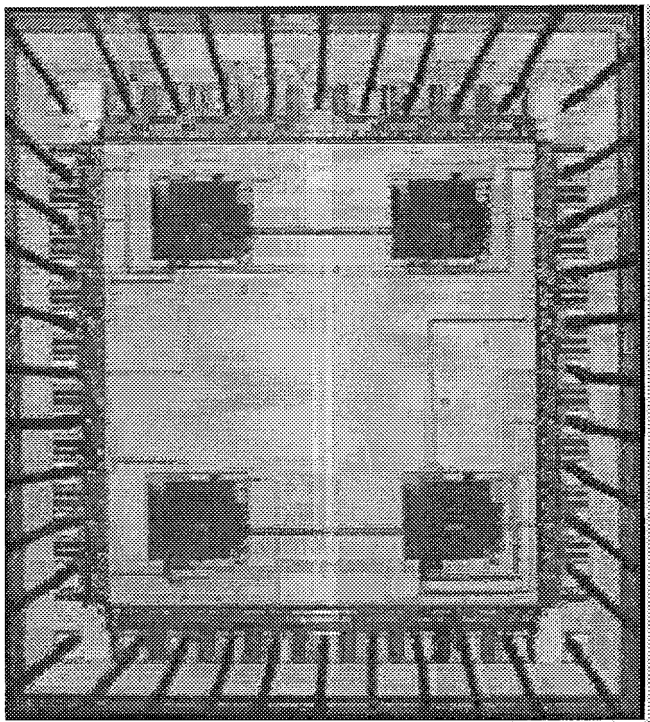


Fig. 11. Microphotograph of the op-amp (four op-amps are on the chip).

TABLE II
DEVIATION OF THE g_m UNDER VARIATIONS OF PROCESS PARAMETERS

Parameter	V_{TON}	V_{TOP}	K_{PN}	K_{PP}
g_m deviation	10%	17%	3%	8%

TABLE III
EXPERIMENTAL RESULTS OF THE OP-AMP

Specifications	Op Amp
Common input range	$V_{ss}+0.08$ to $V_{dd}-0.07$ V
Output swing ($R_l=10k\Omega$)	$V_{ss}+0.04$ to $V_{dd}-0.07$ V
GBW	3.2 MHz
CMRR (DC)	≥ 88 dB
ΔG_m	$\pm 4\%$
Slew rate	5.8 V/ μ s
Input offset voltage	3 mV
Low frequency gain	110 dB
Power dissipation	0.31 mW
Op Amp area	0.12 mm ²

deviation of g_m to within $\pm 4\%$, as shown by the solid line in Fig. 13. The chip-test results are given in Table III.

VI. CONCLUSIONS

An economical but efficient technique to achieve a constant- g_m rail-to-rail complementary N-P differential input stage has been presented. We have demonstrated that dc level shifters can be used to overlap the transition region of the complementary pairs of a differential amplifier. With the proper amount of dc level shift the variation of g_m is within $\pm 5\%$. Simulation also shows that the frequency response of an op-amp using the proposed input stage is independent of the input common-mode voltage. The minimum CMRR is 88 dB, which is acceptable. Finally, measurement demonstrates that the op-amp, with the proposed input stage, allows for rail-to-rail operation.

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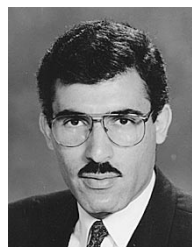
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